

ICM-40609-D Datasheet

TABLE OF CONTENTS

Table of Figures.....	7
Table of Tables.....	7
1 Introduction.....	8
1.1 Purpose and Scope.....	8
1.2 Product Overview.....	8
1.3 Applications.....	8
2 Features.....	9
2.1 Gyroscope Features.....	9
2.2 Accelerometer Features.....	9
2.3 Additional Features.....	9
3 Electrical Characteristics.....	10
3.1 Gyroscope Specifications.....	10
3.2 Accelerometer Specifications.....	11
3.3 Electrical Specifications.....	12
3.4 I ² C Timing Characterization.....	14
3.5 SPI Timing Characterization – 4-Wire SPI Mode.....	15
3.6 SPI Timing Characterization – 3-Wire SPI Mode.....	16
3.7 Absolute Maximum Ratings.....	17
4 Applications Information.....	18
4.1 Pin Out Diagram and Signal Description.....	18
4.2 Typical Operating Circuit.....	19
4.3 Bill of Materials for External Components.....	20
4.4 System Block Diagram.....	21
4.5 Overview.....	21
4.6 Three-Axis MEMS Gyroscope with 16-bit ADCs and Signal Conditioning.....	21
4.7 Three-Axis MEMS Accelerometer with 16-bit ADCs and Signal Conditioning.....	21
4.8 I ² C and SPI Host Interface.....	21
4.9 Self-Test.....	21
4.10 Clocking.....	22
4.11 Sensor Data Registers.....	22
4.12 Interrupts.....	22
4.13 Digital-Output Temperature Sensor.....	22
4.14 Bias and LDOs.....	22
4.15 Charge Pump.....	22
4.16 Standard Power Modes.....	23
5 Signal Path.....	24
5.1 Notch Filter.....	24

5.2	Anti-Alias Filter	25
5.3	User Programmable Offset	27
5.4	UI Filter Block	28
5.5	ODR And FSR Selection	32
6	FIFO	34
6.1	Packet Structure	34
6.2	FIFO Header	35
6.3	Maximum FIFO Storage	36
6.4	FIFO Configuration Registers	36
7	Programmable Interrupts	38
7.1	Wake-On Motion Interrupt	38
8	Digital Interface	39
8.1	I ² C and SPI Serial Interfaces	39
8.2	I ² C Interface	39
8.3	I ² C Communications Protocol	39
8.4	I ² C Terms	41
8.5	SPI Interface	42
9	Assembly	43
9.1	Orientation of Axes	43
9.2	Package Dimensions	44
10	Part Number Package Marking	45
11	Chip Tracking Methodology	46
12	Use Notes	48
12.1	Accelerometer Mode Transitions	48
12.2	Accelerometer Low Power (LP) Mode Averaging Filter Setting	48
12.3	Settings for I ² C, and SPI Operation	48
12.4	Notch Filter and Anti-Alias Filter Operation	48
13	Register Map	49
13.1	User Bank 0 Register Map	49
13.2	User Bank 1 Register Map	50
13.3	User Bank 2 Register Map	50
13.4	User Bank 4 Register Map	51
14	User Bank 0 Register Map – Descriptions	52
14.1	DEVICE_CONFIG	52
14.2	DRIVE_CONFIG	52
14.3	INT_CONFIG	53
14.4	FIFO_CONFIG	53
14.5	TEMP_DATA1	53
14.6	TEMP_DATA0	54
14.7	ACCEL_DATA_X1	54

14.8	ACCEL_DATA_X0	54
14.9	ACCEL_DATA_Y1	54
14.10	ACCEL_DATA_Y0	55
14.11	ACCEL_DATA_Z1	55
14.12	ACCEL_DATA_Z0	55
14.13	GYRO_DATA_X1	55
14.14	GYRO_DATA_X0	55
14.15	GYRO_DATA_Y1	56
14.16	GYRO_DATA_Y0	56
14.17	GYRO_DATA_Z1	56
14.18	GYRO_DATA_Z0	56
14.19	INT_STATUS	57
14.20	FIFO_COUNTH	57
14.21	FIFO_COUNTL	57
14.22	FIFO_DATA	58
14.23	INT_STATUS2	58
14.24	SIGNAL_PATH_RESET	58
14.25	INTF_CONFIG0	59
14.26	INTF_CONFIG1	59
14.27	PWR_MGMT0	60
14.28	GYRO_CONFIG0	61
14.29	ACCEL_CONFIG0	62
14.30	GYRO_CONFIG1	63
14.31	GYRO_ACCEL_CONFIG0	64
14.32	ACCEL_CONFIG1	65
14.33	TMST_CONFIG	65
14.34	WOM_CONFIG	66
14.35	FIFO_CONFIG1	66
14.36	FIFO_CONFIG2	66
14.37	FIFO_CONFIG3	67
14.38	INT_CONFIG0	67
14.39	INT_SOURCE0	68
14.40	INT_SOURCE1	68
14.41	INT_SOURCE3	69
14.42	INT_SOURCE4	69
14.43	FIFO_LOST_PKT0	69
14.44	FIFO_LOST_PKT1	70
14.45	SELF_TEST_CONFIG	70
14.46	OTP_ACCESS	70
14.47	WHO_AM_I	71

14.48	REG_BANK_SEL	71
15	User Bank 1 Register Map – Descriptions	72
15.1	SENSOR_CONFIG0	72
15.2	GYRO_CONFIG_STATIC2	72
15.3	GYRO_CONFIG_STATIC3	72
15.4	GYRO_CONFIG_STATIC4	73
15.5	GYRO_CONFIG_STATIC5	73
15.6	GYRO_CONFIG_STATIC6	73
15.7	GYRO_CONFIG_STATIC7	73
15.8	GYRO_CONFIG_STATIC8	74
15.9	GYRO_CONFIG_STATIC9	74
15.10	GYRO_CONFIG_STATIC10	74
15.11	XG_ST_DATA	75
15.12	YG_ST_DATA	75
15.13	ZG_ST_DATA	75
15.14	TMSTVAL0	75
15.15	TMSTVAL1	76
15.16	TMSTVAL2	76
15.17	OTP_MEM_BANK_SEL	76
15.18	OTP_MEM_START_ADDR	76
15.19	OTP_MEM_READ_WRITE	77
15.20	INTF_CONFIG4	77
15.21	INTF_CONFIG5	77
16	User Bank 2 Register Map – Descriptions	78
16.1	ACCEL_CONFIG_STATIC2	78
16.2	ACCEL_CONFIG_STATIC3	78
16.3	ACCEL_CONFIG_STATIC4	78
16.4	XA_ST_DATA	78
16.5	YA_ST_DATA	79
16.6	ZA_ST_DATA	79
17	User Bank 4 Register Map – Descriptions	80
17.1	ACCEL_WOM_X_THR	80
17.2	ACCEL_WOM_Y_THR	80
17.3	ACCEL_WOM_Z_THR	80
17.4	OFFSET_USER0	80
17.5	OFFSET_USER1	81
17.6	OFFSET_USER2	81
17.7	OFFSET_USER3	81
17.8	OFFSET_USER4	81
17.9	OFFSET_USER5	82

17.10	OFFSET_USER6.....	82
17.11	OFFSET_USER7.....	82
17.12	OFFSET_USER8.....	82
18	Reference.....	83
19	Document Information	84
19.1	Revision History	84

Draft - Advance Information

TABLE OF FIGURES

Figure 1. I ² C Bus Timing Diagram	14
Figure 2. 4-Wire SPI Mode-3 Bus Timing Diagram.....	15
Figure 3. 4-Wire SPI Mode-0 Bus Timing Diagram.....	15
Figure 4. 3-Wire Mode-3 SPI Bus Timing Diagram.....	16
Figure 5. 3-Wire Mode-0 SPI Bus Timing Diagram.....	16
Figure 6. Pin Out Diagram for ICM-40609-D 3x3.0x0.91 mm LGA	18
Figure 7. ICM-40609-D Application Schematic (I ² C Interface to Host).....	19
Figure 8. ICM-40609-D Application Schematic (SPI Interface to Host)	19
Figure 9. ICM-40609-D System Block Diagram.....	21
Figure 10. ICM-40609-D Signal Path	24
Figure 11. FIFO Packet Structure	34
Figure 12. Maximum FIFO Storage	36
Figure 13. START and STOP Conditions	39
Figure 14. Acknowledge on the I ² C Bus	40
Figure 15. Complete I ² C Data Transfer.....	40
Figure 16. Typical SPI Master/Slave Configuration	42
Figure 17. Orientation of Axes of Sensitivity and Polarity of Rotation	43

TABLE OF TABLES

Table 1. Gyroscope Specifications	10
Table 2. Accelerometer Specifications.....	11
Table 3. D.C. Electrical Characteristics	12
Table 4. A.C. Electrical Characteristics.....	13
Table 5. I ² C Timing Characteristics.....	14
Table 6. 4-Wire SPI Timing Characteristics (24-MHz Operation)	15
Table 7. 3-Wire SPI Timing Characteristics (24-MHz Operation)	16
Table 8. Absolute Maximum Ratings	17
Table 9. Signal Descriptions	18
Table 10. Bill of Materials	20
Table 11. Standard Power Modes for ICM-40609-D.....	23
Table 12. I ² C Terms	41

1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This document is a product specification, providing a description, specifications, and design related information on the ICM-40609-D Single-Interface MotionTracking device. The device is housed in a small 3x3x0.91 mm 24-pin LGA package.

1.2 PRODUCT OVERVIEW

The ICM-40609-D is a 6-axis MotionTracking device that combines a 3-axis gyroscope, and a 3-axis accelerometer in a small 3x3x0.91 mm (24-pin LGA) package. It also features a 2K-byte FIFO that can lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. ICM-40609-D, with its 6-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance for consumers.

The gyroscope supports eight programmable full-scale range settings from $\pm 15.625\text{dps}$ to $\pm 2000\text{dps}$, and the accelerometer supports four programmable full-scale range settings from $\pm 4\text{g}$ to $\pm 32\text{g}$.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I²C and SPI serial interfaces, a VDD operating range of 1.71 V to 3.6 V, and a separate VDDIO operating range of 1.71 V to 3.6 V.

The host interface can be configured to support I²C slave or SPI slave modes. The I²C interface supports speeds up to 1 MHz, and the SPI interface supports speeds up to 24 MHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the package size down to a footprint and thickness of 3x3x0.91 mm (24-pin LGA), to provide a very small yet high performance low cost package. The device provides high robustness by supporting 20,000g shock reliability.

1.3 APPLICATIONS

- Drones
- Robotics
- IoT Applications

2 FEATURES

2.1 GYROSCOPE FEATURES

The triple-axis MEMS gyroscope in the ICM-40609-D includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with programmable full-scale range of ± 15.625 , ± 31.25 , ± 62.5 , ± 125 , ± 250 , ± 500 , ± 1000 , and ± 2000 degrees/sec
- Low Noise (LN) power mode support
- Digitally-programmable low-pass filters
- Factory calibrated sensitivity scale factor
- Self-test

2.2 ACCELEROMETER FEATURES

The triple-axis MEMS accelerometer in ICM-40609-D includes a wide range of features:

- Digital-output X-, Y-, and Z-axis accelerometer with programmable full-scale range of $\pm 4g$, $\pm 8g$, $\pm 16g$ and $\pm 32g$
- Low Noise (LN) and Low Power (LP) power modes support
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

2.3 ADDITIONAL FEATURES

ICM-40609-D includes the following additional features:

- 2K byte FIFO buffer enables the applications processor to read the data in bursts
- User-programmable digital filters for gyroscope, accelerometer, and temperature sensor
- Wake on Motion: Detects motion when accelerometer data exceeds a programmable threshold
- 1 MHz I²C / 24 MHz SPI slave host interface
- Digital-output temperature sensor
- Smallest and thinnest LGA package for portable devices: 3x3x0.91 mm (24-pin LGA)
- 20,000 g shock tolerant
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 ELECTRICAL CHARACTERISTICS

3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
GYROSCOPE SENSITIVITY						
Full-Scale Range	GYRO_FS_SEL=0		±2000		°/s	2
	GYRO_FS_SEL =1		±1000		°/s	2
	GYRO_FS_SEL =2		±500		°/s	2
	GYRO_FS_SEL =3		±250		°/s	2
	GYRO_FS_SEL =4		±125		°/s	2
	GYRO_FS_SEL =5		±62.5		°/s	2
	GYRO_FS_SEL =6		±31.25		°/s	2
	GYRO_FS_SEL =7		±15.625		°/s	2
Gyroscope ADC Word Length			16		bits	2
Sensitivity Scale Factor	GYRO_FS_SEL=0		16.4		LSB/(°/s)	2
	GYRO_FS_SEL =1		32.8		LSB/(°/s)	2
	GYRO_FS_SEL =2		65.5		LSB/(°/s)	2
	GYRO_FS_SEL =3		131		LSB/(°/s)	2
	GYRO_FS_SEL =4		262		LSB/(°/s)	2
	GYRO_FS_SEL =5		524.3		LSB/(°/s)	2
	GYRO_FS_SEL =6		1048.6		LSB/(°/s)	2
	GYRO_FS_SEL =7		2097.2		LSB/(°/s)	2
Sensitivity Scale Factor Initial Tolerance	25°C		±0.5		%	1
Sensitivity Scale Factor Variation Over Temperature	-40°C to +85°C	-0.25	±0.045	+0.25	%/°C	3
Nonlinearity	Best fit straight line; 25°C		±0.1		%	3
Cross-Axis Sensitivity			±1		%	3
ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	Board-level, 25°C		±1		°/s	3
ZRO Variation vs. Temperature	-40°C to +85°C		±0.01		°/s/°C	3
OTHER PARAMETERS						
Rate Noise Spectral Density	@ 10 Hz		0.0045		°/s /√Hz	1
Total RMS Noise	Bandwidth = 100 Hz		0.045		°/s-rms	4
Gyroscope Mechanical Frequencies		25	27	29	KHz	1
Low Pass Filter Response	ODR < 1kHz	5		500	Hz	2
	ODR ≥ 1kHz	5		995	Hz	2
Gyroscope Start-Up Time	Time from gyro enable to gyro drive ready		30		ms	3
Output Data Rate		12.5		32000	Hz	2

Table 1. Gyroscope Specifications

Notes:

1. Tested in production.
2. Guaranteed by design.
3. Derived from validation or characterization of parts, not guaranteed in production.
4. Calculated from Rate Noise Spectral Density.

3.2 ACCELEROMETER SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
ACCELEROMETER SENSITIVITY						
Full-Scale Range	ACCEL_FS_SEL =0		±32		g	2
	ACCEL_FS_SEL =1		±16		g	2
	ACCEL_FS_SEL =2		±8		g	2
	ACCEL_FS_SEL =3		±4		g	2
ADC Word Length	Output in two's complement format		16		bits	2
Sensitivity Scale Factor	ACCEL_FS_SEL =0		1,024		LSB/g	2
	ACCEL_FS_SEL =1		2,048		LSB/g	2
	ACCEL_FS_SEL =2		4,096		LSB/g	2
	ACCEL_FS_SEL =3		8,192		LSB/g	2
Sensitivity Scale Factor Initial Tolerance	Component-level		±0.5		%	1
Sensitivity Change vs. Temperature	-40°C to +85°C	-0.12	±0.007	+0.12	%/°C	3
Nonlinearity	Best Fit Straight Line, ±2g		±0.1		%	3
Cross-Axis Sensitivity			±1		%	3
ZERO-G OUTPUT						
Initial Tolerance	Board-level, all axes		±40		mg	3
Zero-G Level Change vs. Temperature	-40°C to +85°C		±0.15		mg/°C	3
OTHER PARAMETERS						
Power Spectral Density	@ 10 Hz		100		μg/√Hz	1
RMS Noise	Bandwidth = 100 Hz		1.00		mg-rms	4
Low-Pass Filter Response	ODR < 1kHz	5		500	Hz	2
	ODR ≥ 1kHz	5		995	Hz	2
Accelerometer Startup Time	From sleep mode to valid data		10		ms	3
Output Data Rate		1.5625		32000	Hz	2

Table 2. Accelerometer Specifications

Notes:

1. Tested in production.
2. Guaranteed by design.
3. Derived from validation or characterization of parts, not guaranteed in production.
4. Calculated from Power Spectral Density.

3.3 ELECTRICAL SPECIFICATIONS

3.3.1 D.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.6	V	1
VDDIO		1.71	1.8	3.6	V	1
SUPPLY CURRENTS						
Low-Noise Mode	6-Axis Gyroscope + Accelerometer		0.77		mA	2
	3-Axis Accelerometer		0.27		mA	2
	3-Axis Gyroscope		0.61		mA	2
Accelerometer Low -Power Mode (Gyroscope disabled)	200Hz ODR, 1x averaging		0.06		mA	2
Full-Chip Sleep Mode	At 25°C		11		μA	2
TEMPERATURE RANGE						
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		+85	°C	1

Table 3. D.C. Electrical Characteristics

Notes:

1. Guaranteed by design.
2. Derived from validation or characterization of parts, not guaranteed in production.

3.3.2 A.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLIES						
Supply Ramp Time	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.01		3	ms	1
Power Supply Noise			10		mV peak-peak	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
25°C Output			0		LSB	3
ADC Resolution			16		bits	2
ODR	With Filter	25		8000	Hz	2
Room Temperature Offset	25°C	-5		5	°C	3
Stabilization Time				14000	μs	2
Sensitivity	Untrimmed		132.48		LSB/°C	1
Sensitivity for FIFO data			2.07		LSB/°C	1
POWER-ON RESET						
Start-up time for register read/write	From power-up			1	ms	1
I ² C ADDRESS						
I ² C ADDRESS	AP_AD0 = 0 AP_AD0 = 1		1101000 1101001			
DIGITAL INPUTS (SCLK, SDI, CS)						
V _{IH} , High Level Input Voltage		0.7*VDDIO			V	1
V _{IL} , Low Level Input Voltage				0.3*VDDIO	V	
C _I , Input Capacitance			< 10		pF	
DIGITAL OUTPUT (SDO, INT1, INT2)						
V _{OH} , High Level Output Voltage	R _{LOAD} =1 MΩ;	0.9*VDDIO			V	1
V _{OL} , LOW-Level Output Voltage	R _{LOAD} =1 MΩ;			0.1*VDDIO	V	
V _{OLINT} , INT Low-Level Output Voltage	OPEN=1, 0.3 mA sink Current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t _{INT} , INT Pulse Width	int_pulse_duration= 0 , 1 (100us, 8us) ;	8		100	μs	
I ² C I/O (SCL, SDA)						
V _{IL} , LOW-Level Input Voltage		-0.5 V		0.3*VDDIO	V	1
V _{IH} , HIGH-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5 V	V	
V _{HYS} , Hysteresis			0.1*VDDIO		V	
V _{OL} , LOW-Level Output Voltage	3 mA sink current	0		0.4	V	
I _{OL} , LOW-Level Output Current	V _{OL} =0.4 V V _{OL} =0.6 V		3 6		mA mA	
Output Leakage Current			100		nA	
t _{of} , Output Fall Time from V _{IHmax} to V _{ILmax}	C _b bus capacitance in pf	20+0.1C _b		300	ns	
INTERNAL CLOCK SOURCE						
Clock Frequency Initial Tolerance	CLKSEL=`2b00 or gyro inactive; 25°C	-3		+3	%	1
	CLK_SEL=`2b01 and gyro active; 25°C	-1		+1	%	1
Frequency Variation over Temperature	CLK_SEL=`2b00 or gyro inactive; -40°C to +85°C			±2	%	1
	CLK_SEL=`2b01 and gyro active; -40°C to +85°C			±2	%	1

Table 4. A.C. Electrical Characteristics

Notes:

1. Expected results based on design, will be updated after characterization. Not guaranteed in production.
2. Guaranteed by design.
3. To be Production tested.

3.4 I²C TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Parameters	Conditions	Min	Typical	Max	Units	Notes
I²C TIMING						
I²C FAST-MODE PLUS						
f _{SCL} , SCL Clock Frequency				1	MHz	1
t _{HD,STA} , (Repeated) START Condition Hold Time		0.26			μs	1
t _{LOW} , SCL Low Period		0.5			μs	1
t _{HIGH} , SCL High Period		0.26			μs	1
t _{SU,STA} , Repeated START Condition Setup Time		0.26			μs	1
t _{HD,DAT} , SDA Data Hold Time		0			μs	1
t _{SU,DAT} , SDA Data Setup Time		50			ns	1
t _r , SDA and SCL Rise Time	C _b bus cap. from 10 to 400 pF			120	ns	1
t _f , SDA and SCL Fall Time	C _b bus cap. from 10 to 400 pF			120	ns	1
t _{SU,STO} , STOP Condition Setup Time		0.5			μs	1
t _{BUF} , Bus Free Time Between STOP and START Condition		0.5			μs	1
C _b , Capacitive Load for each Bus Line			< 400		pF	1
t _{VD,DAT} , Data Valid Time				0.45	μs	1
t _{VD,ACK} , Data Valid Acknowledge Time				0.45	μs	1

Table 5. I²C Timing Characteristics

Notes:

- Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

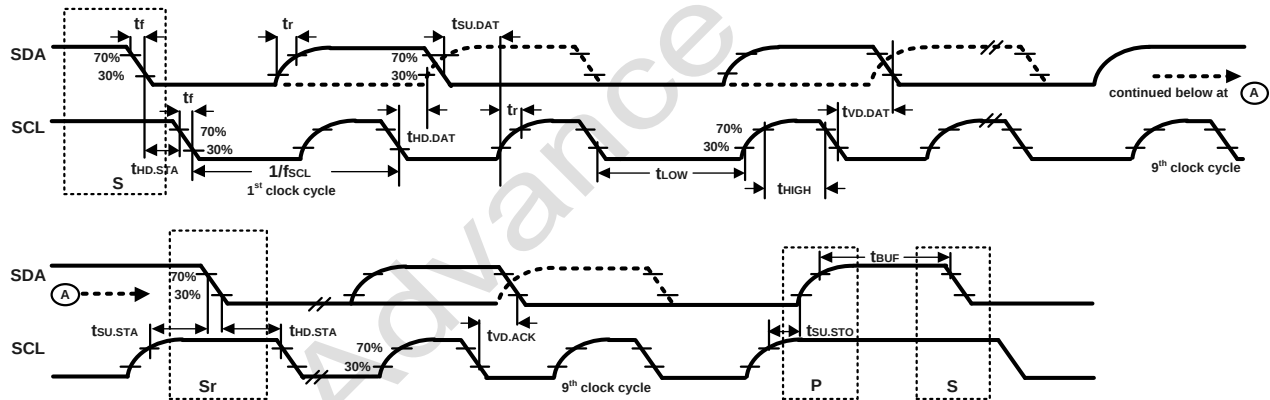


Figure 1. I²C Bus Timing Diagram

3.5 SPI TIMING CHARACTERIZATION – 4-WIRE SPI MODE

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f _{SPC} , SCLK Clock Frequency	Default			24	MHz	1
t _{LOW} , SCLK Low Period		24.5			ns	1
t _{HIGH} , SCLK High Period		24.5			ns	1
t _{SU,CS} , CS Setup Time		39			ns	1
t _{HD,CS} , CS Hold Time		18			ns	1
t _{SU,SDI} , SDI Setup Time		13			ns	1
t _{HD,SDI} , SDI Hold Time		8			ns	1
t _{VD,SDO} , SDO Valid Time	C _{load} = 20 pF			21.5	ns	1
t _{HD,SDO} , SDO Hold Time	C _{load} = 20 pF	9.5			ns	1
t _{DIS,SDO} , SDO Output Disable Time				28	ns	1

Table 6. 4-Wire SPI Timing Characteristics (24-MHz Operation)

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets
2. Based on other parameter values

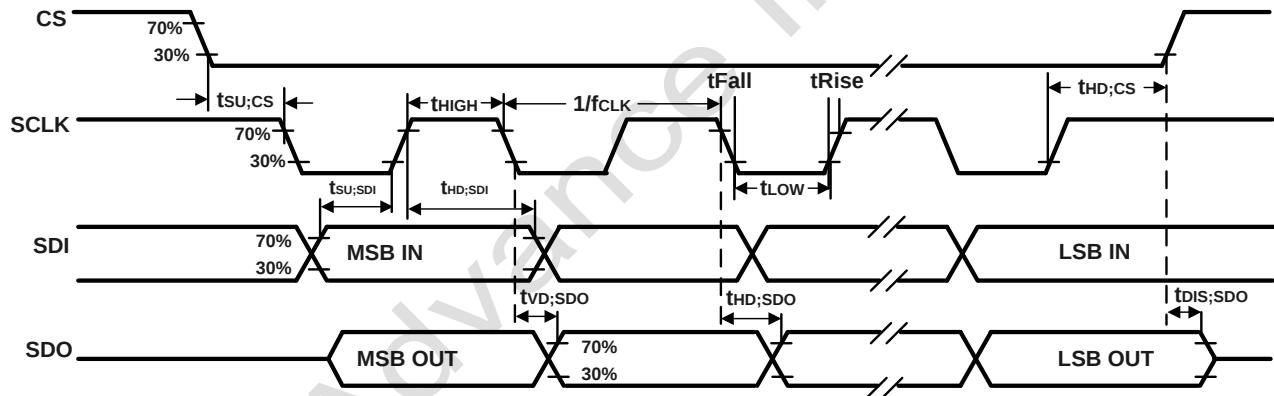


Figure 2. 4-Wire SPI Mode-3 Bus Timing Diagram

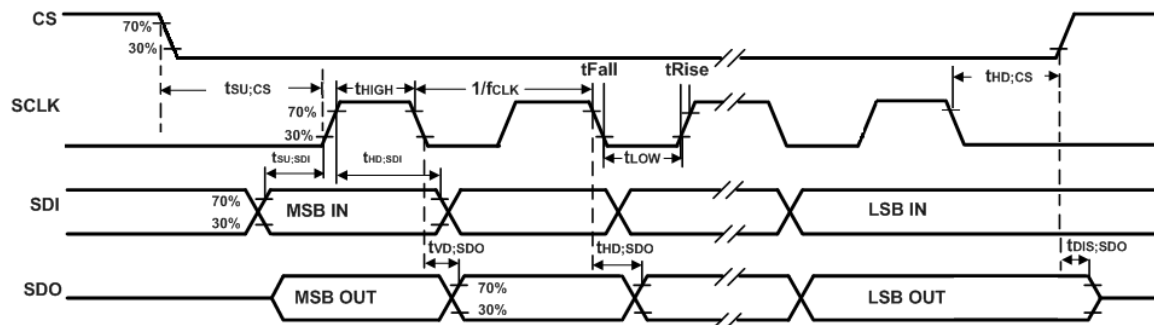


Figure 3. 4-Wire SPI Mode-0 Bus Timing Diagram

3.6 SPI TIMING CHARACTERIZATION – 3-WIRE SPI MODE

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f _{SPC} , SCLK Clock Frequency	Default			24	MHz	1
t _{LOW} , SCLK Low Period		24.5			ns	1
t _{HIGH} , SCLK High Period		24.5			ns	1
t _{SU,CS} , CS Setup Time		39			ns	1
t _{HD,CS} , CS Hold Time		5			ns	1
t _{SU,SDIO} , SDIO Input Setup Time		13			ns	1
t _{HD,SDIO} , SDIO Input Hold Time		8			ns	1
t _{VD,SDIO} , SDIO Output Valid Time	C _{load} = 20 pF			18.5	ns	1
t _{HD,SDIO} , SDIO Output Hold Time	C _{load} = 20 pF	9.5			ns	1
t _{DIS,SDIO} , SDIO Output Disable Time				28	ns	1

Table 7. 3-Wire SPI Timing Characteristics (24-MHz Operation)

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets
2. Based on other parameter values

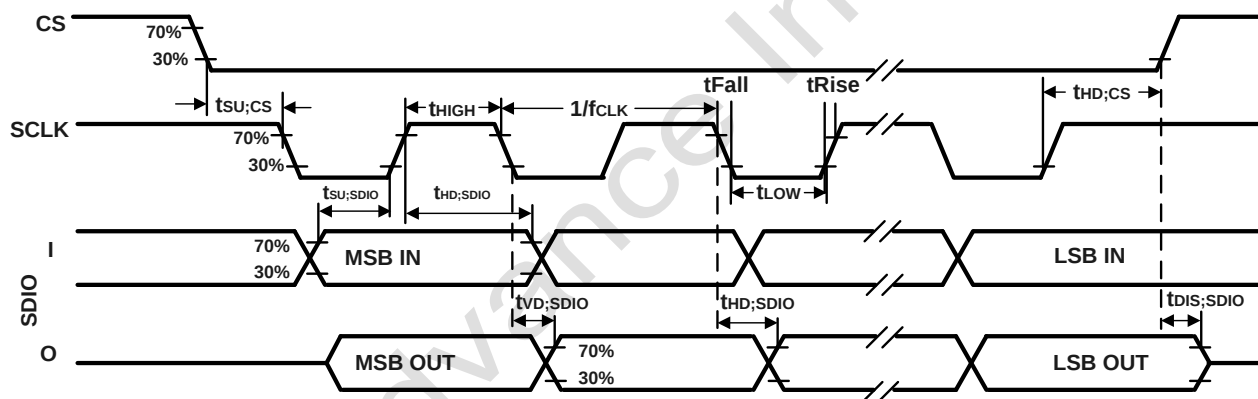


Figure 4. 3-Wire Mode-3 SPI Bus Timing Diagram

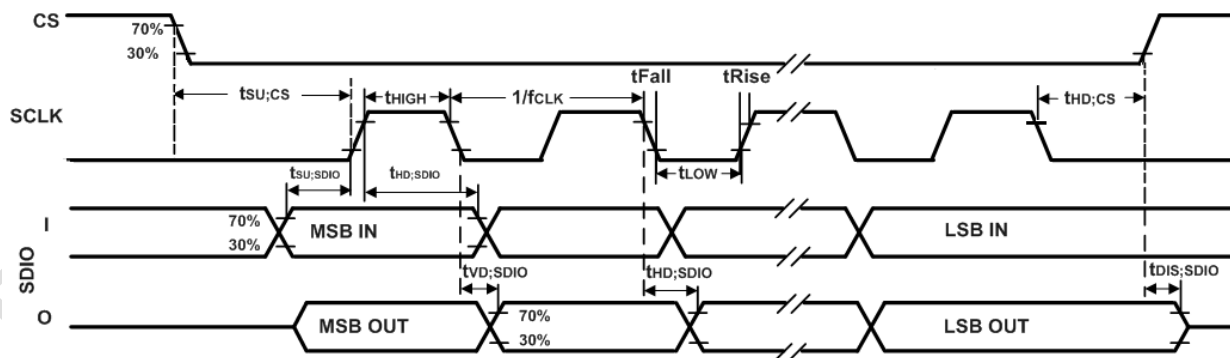


Figure 5. 3-Wire Mode-0 SPI Bus Timing Diagram

3.7 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

Parameter	Rating
Supply Voltage, VDD	-0.5 V to +4 V
Supply Voltage, VDDIO	-0.5 V to +4 V
Input Voltage Level (SCL, SDA)	-0.5 V to VDD + 0.5 V
Acceleration (Any Axis, unpowered)	20,000g for 0.2 ms
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2 kV (HBM); 200 V (MM)
Latch-up	JEDEC Class II (2), 125°C ±100 mA

Table 8. Absolute Maximum Ratings

4 APPLICATIONS INFORMATION

4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
8	VDDIO	Digital I/O supply voltage
9	AD0 / SDO	AD0: I ² C Slave Address LSB SDO: SPI serial data output (4-wire mode)
11	RESV	RESV: Connect to GND
12	INT1 / INT	INT1: Interrupt 1 INT: Interrupt if all interrupts mapped to pin 12
13	VDD	Power supply voltage
18	GND	Power supply ground
19	INT2 / RESV	INT2: Interrupt 2 RESV: Do not connect if all interrupts mapped to pin 12
20	RESV	Reserved, connect to GND
22	nCS	Chip select (SPI mode only)
23	SCL / SCLK	SCL: I ² C serial clock SCLK: SPI serial clock
24	SDA / SDI / SDIO	SDA: I ² C serial data SDI: SPI serial data input (4-wire mode) SDIO: SPI serial data I/O (3-wire mode)
1 – 7, 10, 14 – 17, 21	NC	No Connect pins. Do not connect.

Table 9. Signal Descriptions

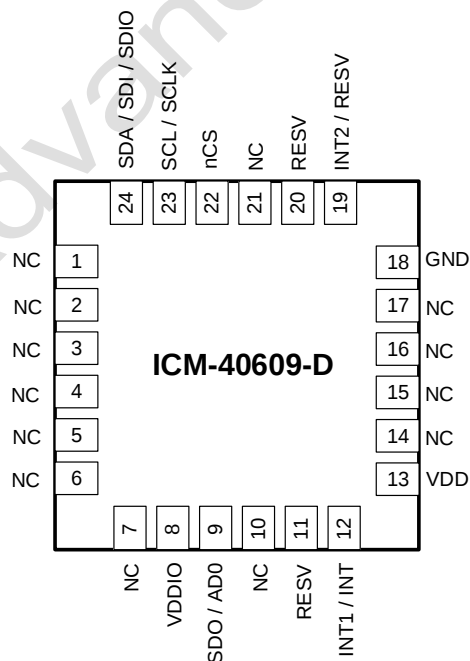


Figure 6. Pin Out Diagram for ICM-40609-D 3x3.0x0.91 mm LGA

4.2 TYPICAL OPERATING CIRCUIT

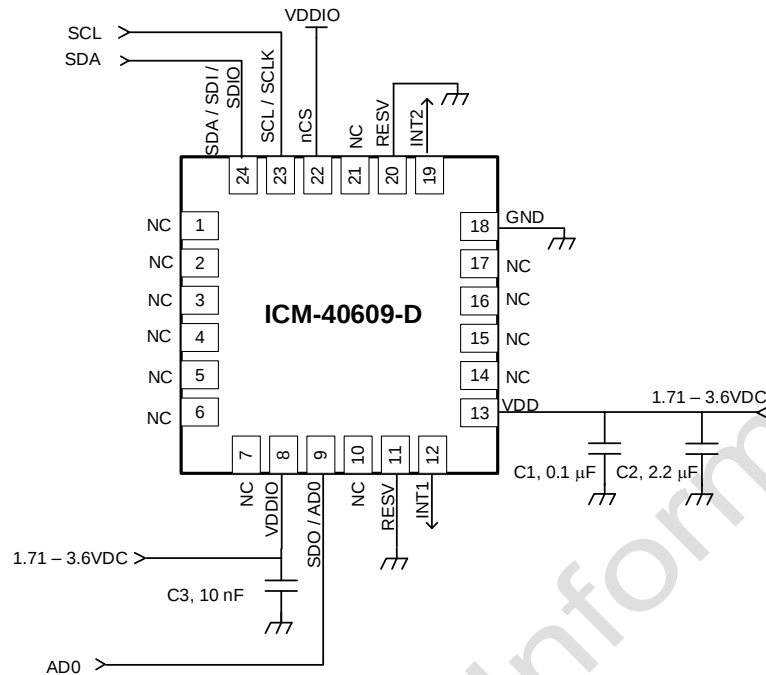


Figure 7. ICM-40609-D Application Schematic (I²C Interface to Host)

Note: I²C lines are open drain and pull-up resistors (e.g. 10 kΩ) are required.

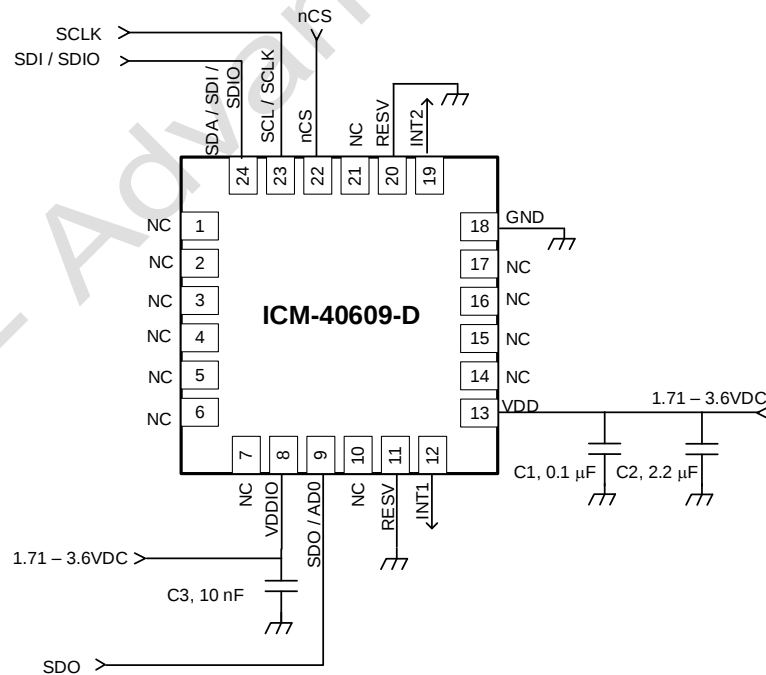


Figure 8. ICM-40609-D Application Schematic (SPI Interface to Host)

4.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

Component	Label	Specification	Quantity
VDD Bypass Capacitors	C1	X7R, 0.1 μ F $\pm$ 10%	1
	C2	X7R, 2.2 μ F $\pm$ 10%	1
VDDIO Bypass Capacitor	C3	X7R, 10nF $\pm$ 10%	1

Table 10. Bill of Materials

4.4 SYSTEM BLOCK DIAGRAM

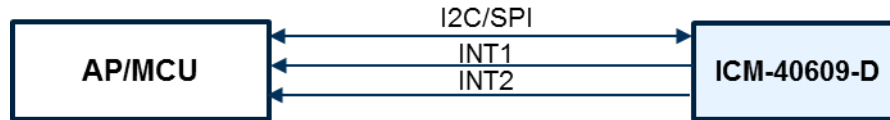


Figure 9. ICM-40609-D System Block Diagram

Note: The above block diagram is an example. Please refer to the pin-out (section 4.1) for other configuration options.

4.5 OVERVIEW

The ICM-40609-D is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- Three-axis MEMS accelerometer sensor with 16-bit ADCs and signal conditioning
- I²C and SPI serial communications interfaces to Host
- Self-Test
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.6 THREE-AXIS MEMS GYROSCOPE WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-40609-D includes a vibratory MEMS rate gyroscope, which detects rotation about the X-, Y-, and Z- Axes. When the gyroscope is rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using on-chip Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ± 15.625 , ± 31.25 , ± 62.5 , ± 125 , ± 250 , ± 500 , ± 1000 , and ± 2000 degrees per second (dps).

4.7 THREE-AXIS MEMS ACCELEROMETER WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-40609-D includes a 3-Axis MEMS accelerometer. Acceleration along a particular axis induces displacement of a proof mass in the MEMS structure, and capacitive sensors detect the displacement. The ICM-40609-D architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0g on the X- and Y-axes and +1g on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. The full scale range of the digital output can be adjusted to $\pm 4g$, $\pm 8g$, $\pm 16g$ and $\pm 32g$.

4.8 I²C AND SPI HOST INTERFACE

The ICM-40609-D communicates to the application processor using an I²C, or SPI serial interface. The ICM-40609-D always acts as a slave when communicating to the application processor.

4.9 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope and accelerometer self-test registers.

When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response.

The self-test response is defined as follows:

Self-test response = Sensor output with self-test enabled – Sensor output with self-test disabled

When the value of the self-test response is within the specified min/max limits of the product specification, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test.

4.10 CLOCKING

The ICM-40609-D has a flexible clocking scheme, allowing the following internal clock sources to be used for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, and various control circuits and registers.

- a) An internal relaxation oscillator
- b) Auto-select between internal relaxation oscillator and gyroscope MEMS oscillator to use the best available source

The only setting supporting specified performance in all modes is option b). It is recommended that option b) be used when using internal clock source.

4.11 SENSOR DATA REGISTERS

The sensor data registers contain the latest gyroscope, accelerometer, and temperature measurement data. They are read-only registers, and are accessed via the serial interface. Data from these registers may be read anytime.

4.12 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the interrupt pins configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); (2) new data is available to be read (from the FIFO and Data registers); (3) accelerometer event interrupts; (4) FIFO watermark; (5) FIFO overflow. The interrupt status can be read from the Interrupt Status register.

4.13 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the ICM-40605 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

Temperature data value from the sensor data registers can be converted to degrees centigrade by using the following formula:

Temperature in Degrees Centigrade = (TEMP_DATA / 132.48) + 25

Temperature data stored in FIFO is an 8-bit quantity, FIFO_TEMP_DATA. It can be converted to degrees centigrade by using the following formula:

Temperature in Degrees Centigrade = (FIFO_TEMP_DATA / 2.07) + 25

4.14 BIAS AND LDOS

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ICM-40609-D.

4.15 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillator.

4.16 STANDARD POWER MODES

The following table lists the user-accessible power modes for ICM-40609-D.

Mode	Name	Gyro	Accel
1	Sleep Mode	Off	Off
2	Standby Mode	Drive On	Off
3	Accelerometer Low-Power Mode	Off	Duty-Cycled
4	Accelerometer Low-Noise Mode	Off	On
5	Gyroscope Low-Noise Mode	On	Off
6	6-Axis Low-Noise Mode	On	On

Table 11. Standard Power Modes for ICM-40609-D

5 SIGNAL PATH

The following figure shows a block diagram of the signal path for ICM-40609-D.

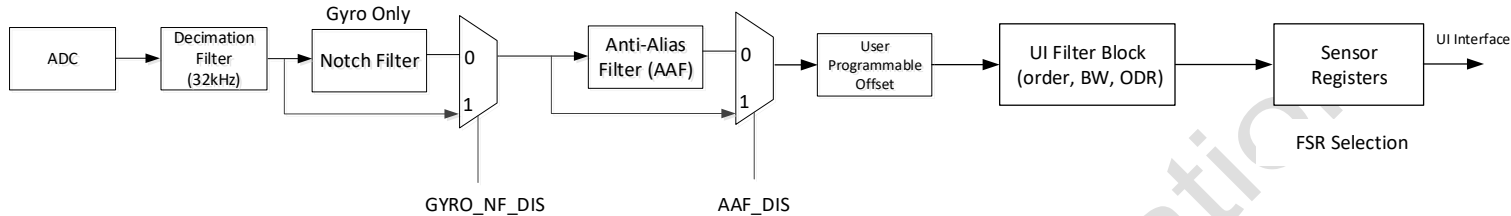


Figure 10. ICM-40609-D Signal Path

The signal path starts with independent 16-bit ADCs for each axis of gyroscope and accelerometer. The ADC output goes through a Decimation Filter that has fixed bandwidth of 32kHz for ICM-40609-D. Other components of the signal path are described below in further detail.

5.1 NOTCH FILTER

The Notch Filter is supported only for the gyroscope signal path. The following steps can be used to program the notch filter. Note that the notch filter is specific to each axis in the gyroscope, so the X, Y and Z axis can be programmed independently.

Frequency of Notch Filter (each axis)

To operate the Notch filter, two parameters NF_COSWZ, and NF_COSWZ_SEL must be programmed for each gyroscope axis.

Parameters NF_COSWZ are defined for each axis of the gyroscope as GYRO_X_NF_COSWZ (register bank 1, register 0x0Fh & register 0x12h), GYRO_Y_NF_COSWZ (register bank 1, register 0x10h & register 0x12h), GYRO_Z_NF_COSWZ (register bank 1, register 0x11h & register 0x12h). Note that the parameters have 9-bit values across two different registers.

Parameters NF_COSWZ_SEL are defined for each axis of the gyroscope as GYRO_X_NF_COSWZ_SEL (register bank 1, register 0x12h, bit 3), GYRO_Y_NF_COSWZ_SEL (register bank 1, register 0x12h, bit 4), GYRO_Z_NF_COSWZ_SEL (register bank 1, register 0x12h, bit 5).

Each value must be calculated using the steps described below, and programmed into the corresponding register locations mentioned above.

$f_{desired}$ is the desired frequency of the Notch Filter in kHz. The lower bound for $f_{desired}$ is 1kHz, and the upper bound is 3kHz. Operating the notch filter outside this range is not supported.

Step1: $COSWZ = \cos(2 * \pi * f_{desired} / 8)$

Step2:

If $\text{abs}(COSWZ) \leq 0.875$

NF_COSWZ = round[COSWZ*256]

NF_COSWZ_SEL = 0

else

NF_COSWZ_SEL = 1

if $COSWZ > 0.875$

NF_COSWZ = round [8*(1-COSWZ)*256]

else if $COSWZ < -0.875$

NF_COSWZ = round [-8*(1+COSWZ)*256]

end

End

Bandwidth of Notch Filter (common to all axes)

The notch filter allows the user to control the width of the notch from eight possible values using a 3-bit parameter GYRO_NF_BW_SEL in register bank 1, register 0x13h, bits 6:4. This parameter is common to all three axes.

GYRO_NF_BW_SEL	Notch Filter Bandwidth (Hz)
0	1449
1	680
2	329
3	162
4	80
5	40
6	20
7	10

The notch filter can be selected or bypassed by using the parameter GYRO_NF_DIS in register bank 1, register 0x0Bh, bit 0 as shown below.

GYRO_NF_DIS	Function
0	Enable notch filter
1	Disable notch filter

5.2 ANTI-ALIAS FILTER

Anti-alias filters for gyroscope and accelerometer can be independently programmed to have bandwidths ranging from 10 Hz to 995 Hz. To program the anti-alias filter for a required bandwidth, use the table below to map the bandwidth to register values as shown:

- Register bank 2, register 0x03h, bits 6:1, ACCEL_AAF_DELT: Code from 1 to 63 that allows programming the bandwidth for accelerometer anti-alias filter
- Register bank 2, register 0x04h, bits 7:0 and Bank 2, register 0x05h, bits 3:0, ACCEL_AAF_DELTSQR: Square of the delt value for accelerometer
- Register bank 2, register 0x05h, bits 7:4, ACCEL_AAF_BITSHIFT: Bitshift value for accelerometer used in hardware implementation
- Register bank 1, register 0x0Ch, bits 5:0, GYRO_AAF_DELT: Code from 1 to 63 that allows programming the bandwidth for gyroscope anti-alias filter
- Register bank 1, register 0x0Dh, bits 7:0 and Bank 1, register 0x0Eh, bits 3:0, GYRO_AAF_DELTSQR: Square of the delt value for gyroscope
- Register bank 1, register 0x0Eh, bits 7:4, GYRO_AAF_BITSHIFT: Bitshift value for gyroscope used in hardware implementation

3dB Bandwidth (Hz)	ACCEL_AAF_DELT; GYRO_AAF_DELT	ACCEL_AAF_DELTSQR; GYRO_AAF_DELTSQR	ACCEL_AAF_BITSHIFT; GYRO_AAF_BITSHIFT
42	1	1	15
84	2	4	13

126	3	9	12
170	4	16	11
213	5	25	10
258	6	36	10
303	7	49	9
348	8	64	9
394	9	81	9
441	10	100	8
488	11	122	8
536	12	144	8
585	13	170	8
634	14	196	7
684	15	224	7
734	16	256	7
785	17	288	7
837	18	324	7
890	19	360	6
943	20	400	6
997	21	440	6
1051	22	488	6
1107	23	528	6
1163	24	576	6
1220	25	624	6
1277	26	680	6
1336	27	736	5
1395	28	784	5
1454	29	848	5
1515	30	896	5
1577	31	960	5
1639	32	1024	5
1702	33	1088	5
1766	34	1152	5
1830	35	1232	5
1896	36	1296	5
1962	37	1376	4
2029	38	1440	4
2097	39	1536	4
2166	40	1600	4
2235	41	1696	4
2306	42	1760	4
2377	43	1856	4
2449	44	1952	4
2522	45	2016	4
2596	46	2112	4

2671	47	2208	4
2746	48	2304	4
2823	49	2400	4
2900	50	2496	4
2978	51	2592	4
3057	52	2720	4
3137	53	2816	3
3217	54	2944	3
3299	55	3008	3
3381	56	3136	3
3464	57	3264	3
3548	58	3392	3
3633	59	3456	3
3718	60	3584	3
3805	61	3712	3
3892	62	3840	3
3979	63	3968	3

The anti-alias filter can be selected or bypassed for the gyroscope by using the parameter GYRO_AAF_DIS in register bank 1, register 0x0Bh, bit 1 as shown below.

GYRO_AAF_DIS	Function
0	Enable gyroscope anti-aliasing filter
1	Disable gyroscope anti-aliasing filter

The anti-alias filter can be selected or bypassed for the accelerometer by using the parameter ACCEL_AAF_DIS in register bank 2, register 0x03h, bit 0 as shown below.

ACCEL_AAF_DIS	Function
0	Enable accelerometer anti-aliasing filter
1	Disable accelerometer anti-aliasing filter

5.3 USER PROGRAMMABLE OFFSET

Gyroscope and accelerometer offsets can be programmed by the user by using registers OFFSET_USER0, through OFFSET_USER8, in bank 0, registers 0x77h through 0x7Fh (bank 4) as shown below.

Register Address	Register Name	Bits	Function
0x77h	OFFSET_USER0	7:0	Lower bits of X-gyro offset programmed by user. Max value is ± 64 dps, resolution is 1/32 dps.
0x78h	OFFSET_USER1	3:0	Upper bits of X-gyro offset programmed by user. Max value is ± 64 dps, resolution is 1/32 dps.
		7:4	Upper bits of Y-gyro offset programmed by user. Max value is ± 64 dps, resolution is 1/32 dps.
0x79h	OFFSET_USER2	7:0	Lower bits of Y-gyro offset programmed by user. Max value is ± 64 dps, resolution is 1/32 dps.

0x7Ah	OFFSET_USER3	7:0	Lower bits of Z-gyro offset programmed by user. Max value is ± 64 dps, resolution is 1/32 dps.
0x7Bh	OFFSET_USER4	3:0	Upper bits of Z-gyro offset programmed by user. Max value is ± 64 dps, resolution is 1/32 dps.
		7:4	Upper bits of X-accel offset programmed by user. Max value is ± 1 g, resolution is 0.5 g.
0x7Ch	OFFSET_USER5	7:0	Lower bits of X-accel offset programmed by user. Max value is ± 1 g, resolution is 0.5 g.
0x7Dh	OFFSET_USER6	7:0	Lower bits of Y-accel offset programmed by user. Max value is ± 1 g, resolution is 0.5 g.
0x7Eh	OFFSET_USER7	3:0	Upper bits of Y-accel offset programmed by user. Max value is ± 1 g, resolution is 0.5 g.
		7:4	Upper bits of Z-accel offset programmed by user. Max value is ± 1 g, resolution is 0.5 g.
0x7Fh	OFFSET_USER8	7:0	Lower bits of Z-accel offset programmed by user. Max value is ± 1 g, resolution is 0.5 g.

5.4 UI FILTER BLOCK

The UI filter block can be programmed to select filter order and bandwidth independently for gyroscope and accelerometer.

Gyroscope filter order can be selected by programming the parameter GYRO_UI_FILT_ORD in register bank 0, register 0x51h, bits 3:2, as shown below.

GYRO_UI_FILT_ORD	Filter Order
00	1 st order
01	2 nd order
10	3 rd order
11	Reserved

Accelerometer filter order can be selected by programming the parameter ACCEL_UI_FILT_ORD in register bank 0, register 0x53h, bits 4:3, as shown below.

ACCEL_UI_FILT_ORD	Filter Order
00	1 st order
01	2 nd order
10	3 rd order
11	Reserved

Gyroscope and accelerometer filter 3dB bandwidth can be selected by programming the parameter GYRO_UI_FILT_BW in register bank 0, register 0x52h, bits 3:0, and the parameter ACCEL_UI_FILT_BW in register bank 0, register 0x52h, bits 7:4, as shown below. The values shown in bold correspond to low noise and the values shown in *italics* correspond to low latency. User can select the appropriate setting based on the application requirements for power and latency. Corresponding Noise Bandwidth (NBW) and Group Delay values are also shown.

1st Order Filter 3dB Bandwidth, Noise Bandwidth (NBW), Group Delay

3dB Bandwidth (Hz) for GYRO/ACCEL_UI_FILT_ORD=0 (1st order filter)											
		GYRO/ACCEL_UI_FILT_BW									
GYRO/ACCEL_ODR	ODR(Hz)	0	1	2	3	4	5	6	7	14	15

1	32000	8400.0									
2	16000	4194.1									
3	8000	2096.3									
4	4000	1048.1									
5	2000	524.0									
6	1000	498.3	227.2	188.9	111.0	92.4	59.6	48.8	23.9	262.0	2096.3
15	500	249.1	113.6	94.4	55.5	46.2	29.8	24.4	11.9	131.0	1048.1
7	200	99.6	90.9	75.5	44.4	37.0	23.8	19.5	9.6	104.8	419.2
8	100	49.8	90.9	75.5	44.4	37.0	23.8	19.5	9.6	104.8	209.6
9	50	24.9	90.9	75.5	44.4	37.0	23.8	19.5	9.6	104.8	104.8
10	25	12.5	90.9	75.5	44.4	37.0	23.8	19.5	9.6	104.8	52.4
11	12.5	12.5	90.9	75.5	44.4	37.0	23.8	19.5	9.6	104.8	52.4

		NBW Bandwidth (Hz) for GYRO/ACCEL_UI_FILT_ORD=0 (1st order filter)									
		GYRO/ACCEL_UI_FILT_BW									
GYRO/ACCEL_ODR	ODR(Hz)	0	1	2	3	4	5	6	7	14	15
1	32000	8831.7									
2	16000	4410.6									
3	8000	2204.6									
4	4000	1102.2									
5	2000	551.1									
6	1000	551.1	230.8	196.3	126.5	108.9	75.8	64.1	34.1	275.6	2204.6
15	500	280.5	115.4	98.2	63.3	54.5	37.9	32.1	17.1	137.8	1102.2
7	200	112.2	92.4	78.5	50.6	43.6	30.3	25.7	13.7	110.3	440.9
8	100	56.1	92.4	78.5	50.6	43.6	30.3	25.7	13.7	110.3	220.5
9	50	28.1	92.4	78.5	50.6	43.6	30.3	25.7	13.7	110.3	110.3
10	25	14.1	92.4	78.5	50.6	43.6	30.3	25.7	13.7	110.3	55.2
11	12.5	14.1	92.4	78.5	50.6	43.6	30.3	25.7	13.7	110.3	55.2

		Group Delay @DC (ms) for GYRO/ACCEL_UI_FILT_ORD=0 (1st order filter)									
		GYRO/ACCEL_UI_FILT_BW									
GYRO/ACCEL_ODR	ODR(Hz)	0	1	2	3	4	5	6	7	14	15
1	32000	0.1									
2	16000	0.1									
3	8000	0.2									
4	4000	0.4									
5	2000	0.8									
6	1000	0.6	1.8	2.0	2.8	3.1	4.1	4.7	8.1	1.5	0.2
15	500	1.1	3.6	4.0	5.5	6.1	8.1	9.3	16.2	3.0	0.4
7	200	2.7	4.4	5.0	6.8	7.6	10.2	11.7	20.3	3.8	1.0
8	100	5.3	4.4	5.0	6.8	7.6	10.2	11.7	20.3	3.8	1.9
9	50	10.5	4.4	5.0	6.8	7.6	10.2	11.7	20.3	3.8	3.8
10	25	21.0	4.4	5.0	6.8	7.6	10.2	11.7	20.3	3.8	7.5
11	12.5	21.0	4.4	5.0	6.8	7.6	10.2	11.7	20.3	3.8	7.5

2nd Order Filter 3dB Bandwidth, Noise Bandwidth (NBW), Group Delay

		3dB Bandwidth (Hz) for GYRO/ACCEL_UI_FILT_ORD=1 (2nd order filter)									
		GYRO/ACCEL_UI_FILT_BW									
GYRO/ACCEL_ODR	ODR(Hz)	0	1	2	3	4	5	6	7	14	15
1	32000	8400.0									
2	16000	4194.1									
3	8000	2096.3									
4	4000	1048.1									
5	2000	524.0									
6	1000	493.3	230.7	191.6	117.5	97.1	59.6	48.0	21.3	262.0	2096.3
15	500	246.7	115.3	95.8	58.8	48.5	29.8	24.0	10.6	131.0	1048.1
7	200	98.7	92.3	76.6	47.0	38.8	23.8	19.2	8.5	104.8	419.2
8	100	49.3	92.3	76.6	47.0	38.8	23.8	19.2	8.5	104.8	209.6
9	50	24.7	92.3	76.6	47.0	38.8	23.8	19.2	8.5	104.8	104.8
10	25	12.3	92.3	76.6	47.0	38.8	23.8	19.2	8.5	104.8	52.4
11	12.5	12.3	92.3	76.6	47.0	38.8	23.8	19.2	8.5	104.8	52.4

		NBW Bandwidth (Hz) for GYRO/ACCEL_UI_FILT_ORD=1 (2nd order filter)									
		GYRO/ACCEL_UI_FILT_BW									
GYRO/ACCEL_ODR	ODR(Hz)	0	1	2	3	4	5	6	7	14	15
1	32000	8831.7									
2	16000	4410.6									
3	8000	2204.6									
4	4000	1102.2									
5	2000	551.1									
6	1000	551.1	223.7	189.9	122.7	102.8	64.7	52.5	23.7	275.6	2204.6
15	500	259.6	111.9	95.0	61.4	51.4	32.4	26.3	11.9	137.8	1102.2
7	200	103.9	89.5	76.0	49.1	41.2	25.9	21.0	9.5	110.3	440.9
8	100	52.0	89.5	76.0	49.1	41.2	25.9	21.0	9.5	110.3	220.5
9	50	26.0	89.5	76.0	49.1	41.2	25.9	21.0	9.5	110.3	110.3
10	25	13.0	89.5	76.0	49.1	41.2	25.9	21.0	9.5	110.3	55.2
11	12.5	13.0	89.5	76.0	49.1	41.2	25.9	21.0	9.5	110.3	55.2

		Group Delay @DC (ms) for GYRO/ACCEL_UI_FILT_ORD=1 (2nd order filter)									
		GYRO/ACCEL_UI_FILT_BW									
GYRO/ACCEL_ODR	ODR(Hz)	0	1	2	3	4	5	6	7	14	15
1	32000	0.1									
2	16000	0.1									
3	8000	0.2									
4	4000	0.4									
5	2000	0.8									
6	1000	0.7	2.1	2.4	3.2	3.7	5.2	6.1	12.0	1.5	0.2
15	500	1.3	4.1	4.7	6.4	7.3	10.4	12.2	24.0	3.0	0.4
7	200	3.3	5.1	5.8	8.0	9.1	12.9	15.3	30.0	3.8	1.0

8	100	6.5	5.1	5.8	8.0	9.1	12.9	15.3	30.0	3.8	1.9
9	50	12.9	5.1	5.8	8.0	9.1	12.9	15.3	30.0	3.8	3.8
10	25	25.7	5.1	5.8	8.0	9.1	12.9	15.3	30.0	3.8	7.5
11	12.5	25.7	5.1	5.8	8.0	9.1	12.9	15.3	30.0	3.8	7.5

3rd Order Filter 3dB Bandwidth, Noise Bandwidth (NBW), Group Delay

		3dB Bandwidth (Hz) for GYRO/ACCEL_UI_FILT_ORD=2 (3rd order filter)									
		GYRO/ACCEL_UI_FILT_BW									
GYRO/ACCEL_ODR	ODR(Hz)	0	1	2	3	4	5	6	7	14	15
1	32000	8400.0									
2	16000	4194.1									
3	8000	2096.3									
4	4000	1048.1									
5	2000	524.0									
6	1000	492.9	234.7	195.8	118.9	97.9	60.8	46.8	25.2	262.0	2096.3
15	500	246.4	117.4	97.9	59.5	48.9	30.4	23.4	12.6	131.0	1048.1
7	200	98.6	93.9	78.3	47.6	39.2	24.3	18.7	10.1	104.8	419.2
8	100	49.3	93.9	78.3	47.6	39.2	24.3	18.7	10.1	104.8	209.6
9	50	24.6	93.9	78.3	47.6	39.2	24.3	18.7	10.1	104.8	104.8
10	25	12.3	93.9	78.3	47.6	39.2	24.3	18.7	10.1	104.8	52.4
11	12.5	12.3	93.9	78.3	47.6	39.2	24.3	18.7	10.1	104.8	52.4

		NBW Bandwidth (Hz) for GYRO/ACCEL_UI_FILT_ORD=0 (1st order filter)									
		GYRO/ACCEL_UI_FILT_BW									
GYRO/ACCEL_ODR	ODR(Hz)	0	1	2	3	4	5	6	7	14	15
1	32000	8831.7									
2	16000	4410.6									
3	8000	2204.6									
4	4000	1102.2									
5	2000	551.1									
6	1000	551.1	221.3	188.5	120.1	100.0	62.9	48.6	26.4	275.6	2204.6
15	500	252.0	110.7	94.3	60.1	50.0	31.5	24.3	13.2	137.8	1102.2
7	200	100.8	88.6	75.4	48.1	40.0	25.2	19.5	10.6	110.3	440.9
8	100	50.4	88.6	75.4	48.1	40.0	25.2	19.5	10.6	110.3	220.5
9	50	25.2	88.6	75.4	48.1	40.0	25.2	19.5	10.6	110.3	110.3
10	25	12.6	88.6	75.4	48.1	40.0	25.2	19.5	10.6	110.3	55.2
11	12.5	12.6	88.6	75.4	48.1	40.0	25.2	19.5	10.6	110.3	55.2

		Group Delay @DC (ms) for GYRO/ACCEL_UI_FILT_ORD=2 (3rd order filter)									
		GYRO/ACCEL_UI_FILT_BW									
GYRO/ACCEL_ODR	ODR(Hz)	0	1	2	3	4	5	6	7	14	15
1	32000	0.1									
2	16000	0.1									
3	8000	0.2									

4	4000	0.4									
5	2000	0.8									
6	1000	0.8	2.3	2.7	4.0	4.6	6.6	8.2	14.1	1.5	0.2
15	500	1.6	4.6	5.4	7.9	9.2	13.2	16.3	28.1	3.0	0.4
7	200	4.0	5.8	6.8	9.8	11.4	16.5	20.4	35.2	3.8	1.0
8	100	8.0	5.8	6.8	9.8	11.4	16.5	20.4	35.2	3.8	1.9
9	50	15.9	5.8	6.8	9.8	11.4	16.5	20.4	35.2	3.8	3.8
10	25	31.8	5.8	6.8	9.8	11.4	16.5	20.4	35.2	3.8	7.5
11	12.5	31.8	5.8	6.8	9.8	11.4	16.5	20.4	35.2	3.8	7.5

5.5 ODR AND FSR SELECTION

Gyroscope ODR can be selected by programming the parameter GYRO_ODR in register bank 0, register 0x4Fh, bits 3:0 as shown below.

GYRO_ODR	Gyroscope ODR Value
0000	Reserved
0001	32kHz
0010	16kHz
0011	8kHz
0100	4kHz
0101	2kHz
0110	1kHz (default)
0111	200Hz
1000	100Hz
1001	50Hz
1010	25Hz
1011	12.5Hz
1100	Reserved
1101	Reserved
1110	Reserved
1111	500Hz

Gyroscope FSR can be selected by programming the parameter GYRO_FS_SEL in register bank 0, register 0x4Fh, bits 7:5 as shown below.

GYRO_FS_SEL	Gyroscope FSR Value
000	±2000dps
001	±1000dps
010	±500dps
011	±250dps
100	±125dps
101	±62.5dps

110	±31.25dps
111	±15.625dps

Accelerometer ODR can be selected by programming the parameter ACCEL_ODR in register bank 0, register 0x50h, bits 3:0 as shown below.

ACCEL_ODR	Accelerometer ODR Value
0000	Reserved
0001	32kHz
0010	16kHz
0011	8kHz
0100	4kHz
0101	2kHz
0110	1kHz (default)
0111	200Hz
1000	100Hz
1001	50Hz
1010	25Hz
1011	12.5Hz
1100	6.25Hz
1101	3.125Hz
1110	1.5625Hz
1111	500Hz

Accelerometer FSR can be selected by programming the parameter ACCEL_FS_SEL in register bank 0, register 0x50h, bits 7:5 as shown below.

ACCEL_FS_SEL	Accelerometer FSR Value
000	±32g
001	±16g
010	±8g
011	±4g
100	Reserved
101	Reserved
110	Reserved
111	Reserved

6 FIFO

The ICM-40609-D contains a 2K byte FIFO register that is accessible via the serial interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyroscope data, accelerometer data, and temperature readings. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO.

6.1 PACKET STRUCTURE

The following figure shows the FIFO packet structures supported in ICM-40609-D.

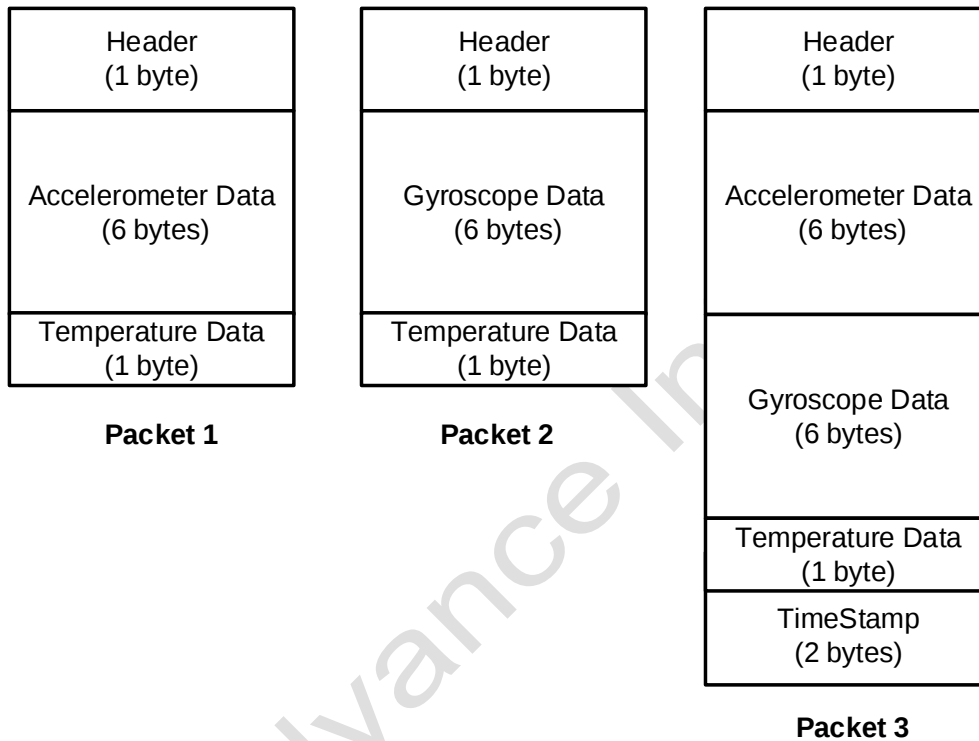


Figure 11. FIFO Packet Structure

The rest of this sub-section describes how individual data is packaged in the different FIFO packet structures.

Packet 1: Individual data is packaged in Packet 1 as shown below.

Byte	Content
0x00	FIFO Header
0x01	Accel X [15:8]
0x02	Accel X [7:0]
0x03	Accel Y [15:8]
0x04	Accel Y [7:0]
0x05	Accel Z [15:8]
0x06	Accel Z [7:0]
0x07	Temperature[7:0]

Packet 2: Individual data is packaged in Packet 2 as shown below.

Byte	Content
0x00	FIFO Header
0x01	Gyro X [15:8]
0x02	Gyro X [7:0]
0x03	Gyro Y [15:8]
0x04	Gyro Y [7:0]
0x05	Gyro Z [15:8]
0x06	Gyro Z [7:0]
0x07	Temperature[7:0]

Packet 3: Individual data is packaged in Packet 3 as shown below.

Byte	Content
0x00	FIFO Header
0x01	Accel X [15:8]
0x02	Accel X [7:0]
0x03	Accel Y [15:8]
0x04	Accel Y [7:0]
0x05	Accel Z [15:8]
0x06	Accel Z [7:0]
0x07	Gyro X [15:8]
0x08	Gyro X [7:0]
0x09	Gyro Y [15:8]
0x0A	Gyro Y [7:0]
0x0B	Gyro Z [15:8]
0x0C	Gyro Z [7:0]
0x0D	Temperature[7:0]
0x0E	TimeStamp[15:8]
0x0F	TimeStamp[7:0]

6.2 FIFO HEADER

The following table shows the structure of the 1 byte FIFO header.

Bit Field	Item	Description
7	HEADER_MSG	1: FIFO is empty 0: Packet contains sensor data
6	HEADER_ACCEL	1: Packet is sized so that accel data have location in the packet, FIFO_ACCEL_EN must be 1 0: Packet does not contain accel sample
5	HEADER_GYRO	1: Packet is sized so that gyro data have location in the packet, FIFO_GYRO_EN must be 1 0: Packet does not contain gyro sample
3:2	HEADER_TIMESTAMP	00: Packet does not contain timestamp 01: Reserved 10: Packet contains ODR Timestamp

		11: Reserved
1	HEADER_ODR_ACCEL	1: The ODR for accel is different for this accel data packet compared to the previous accel packet 0: The ODR for accel is the same as the previous packet with accel
0	HEADER_ODR_GYRO	1: The ODR for gyro is different for this gyro data packet compared to the previous accel packet 0: The ODR for gyro is the same as the previous packet with accel

Note at least HEADER_ACCEL or HEADER_GYRO must be set for a sensor data packet to be set.

6.3 MAXIMUM FIFO STORAGE

The maximum number of packets that can be stored in FIFO is a variable quantity depending on the use case. As shown in the figure below, the physical FIFO size is 2048 bytes. A number of bytes equal to the packet size selected (see section 6.1) is reserved to prevent reading a packet during write operation. Additionally, a read cache 2 packets wide is available.

When there is no serial interface operation, the read cache is not available for storing packets, being fed by the serial interface clock.

When serial interface operation happens, depending on the operation length and the packet size chosen, either 1 or 2 of the packet entries in read cache may become available for storing packets. In that case the total storage available is up to the maximum number of packets that can be accommodated in 2048 bytes + 1 packet size, depending on the packet size used.

Due to the non-deterministic nature of system operation, driver memory allocation should always be the largest size of 2080 bytes.

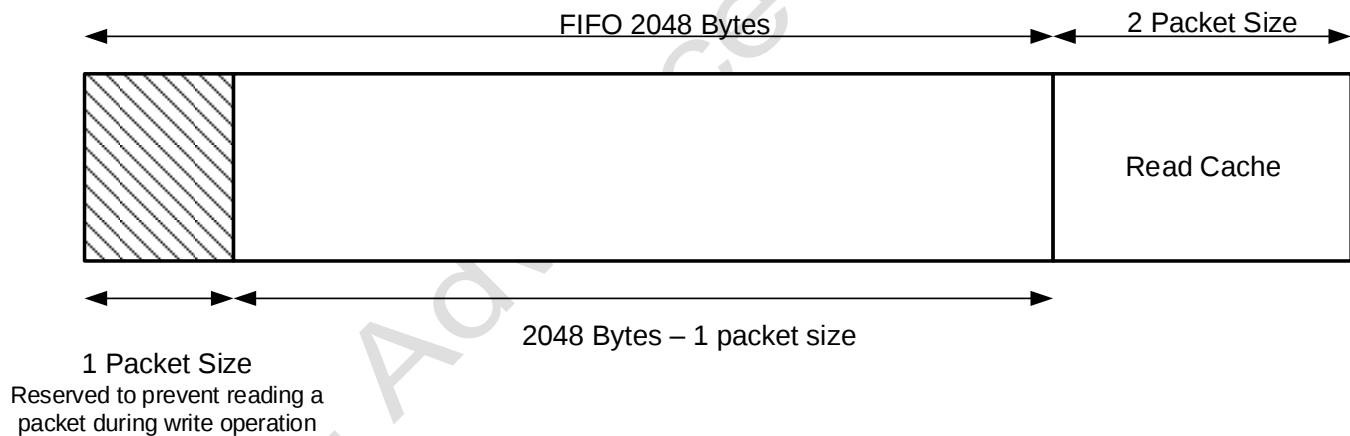


Figure 12. Maximum FIFO Storage

6.4 FIFO CONFIGURATION REGISTERS

The following control bits in bank 0, register 0x5Fh determine what data is placed into the FIFO. The values of these bits may change while the FIFO is being filled without corruption of the FIFO.

BIT	NAME	FUNCTION
3	FIFO_TMST_EN	0: FIFO will only contain ODR timestamp information 1: Reserved
1	FIFO_GYRO_EN	0: Default setting; Gyroscope data not placed into FIFO 1: Enables gyroscope data packets of 6-bytes to be placed in FIFO
0	FIFO_ACCEL_EN	0: Default setting; Accelerometer data not placed into FIFO 1: Enables accelerometer data packets of 6-bytes to be placed in FIFO

Configuration register settings above impact FIFO header and FIFO packet size as follows:

FIFO_ACCEL_EN	FIFO_GYRO_EN	FIFO_TMST_EN	Header	Packet size
1	1	0	8'b_0110_10xx	16 Bytes
1	1	1	8'b_0110_1xxx	16 Bytes
1	0	X	8'b_0100_00xx	8 Bytes
0	1	X	8'b_0010_00xx	8 Bytes
0	0	X	No FIFO writes	No FIFO writes

7 PROGRAMMABLE INTERRUPTS

The ICM-40609-D has a programmable interrupt system that can generate an interrupt signal on the INT pins. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually. There are two interrupt outputs. Any interrupt may be mapped to either interrupt pin as explained in the register section. The following configuration options are available for the interrupts

- INT1 and INT2 can be push-pull or open drain
- Level or pulse mode
- Active high or active low

7.1 WAKE-ON MOTION INTERRUPT

The ICM-40609-D provides motion detection capability. A qualifying motion sample is one where the high passed sample from any axis has an absolute value exceeding a user-programmable threshold. The following steps explain how to configure the Wake-on-Motion Interrupt.

- Wake on Motion configuration parameters
 1. WOM_X_TH (Register 0x4Ah in Bank 4)
 2. WOM_Y_TH (Register 0x4Bh in Bank 4)
 3. WOM_Z_TH (Register 0x4Ch in Bank 4)
 4. WOM_INT_MODE (Register 0x57h in Bank 0)
 5. WOM_MODE (Register 0x57h in Bank 0)
 6. WOM_MODE1 (Register 0x57h in Bank 0)
- Initialize Sensor in a typical configuration
 1. Set accelerometer ODR (Register 0x50h in Bank 0)
ACCEL_ODR = 9 for 50 Hz
 2. Set Accel to Low Power mode (Register 0x4Eh in Bank 0)
ACCEL_MODE = 2 and (Register 0x4Dh in Bank 0), ACCEL_LP_CLK_SEL = 0, for low power mode
 3. Wait 1 millisecond
- Initialize Wake on Motion hardware
 1. Set WOM_X_TH to 98 (Register 0x4Ah in Bank 4)
 2. Set WOM_Y_TH to 98 (Register 0x4Bh in Bank 4)
 3. Set WOM_Z_TH to 98 (Register 0x4Ch in Bank 4)
 4. Wait 1 millisecond
 5. Set WOM_INT_MODE to 0 (Register 0x57h in Bank 0)
 6. Set WOM_MODE to 1 (Register 0x57h in Bank 0)
 7. Set WOM_MODE1 to 1 (Register 0x57h in Bank 0)
 8. Wait 1 millisecond
 9. Enable all 3 axes as WOM sources for INT1 by setting bits 2:0 in register INT_SOURCE1 (Register 0x66h in Bank 0) to 1. Or if INT2 is selected for WOM, enable all 3 axes as WOM sources by setting bits 2:0 in register INT_SOURCE4 (Register 0x69h in Bank 0) to 1.
 10. Wait 50 milliseconds
- Output registers
 1. Read interrupt register (Register 0x37h in Bank 0) for WOM_X_INT
 2. Read interrupt register (Register 0x37h in Bank 0) for WOM_Y_INT
 3. Read interrupt register (Register 0x37h in Bank 0) for WOM_Z_INT

8 DIGITAL INTERFACE

8.1 I²C AND SPI SERIAL INTERFACES

The internal registers and memory of the ICM-40609-D can be accessed using I²C at 1 MHz or SPI at 24 MHz. SPI operates in 3-wire or 4-wire mode. Pin assignments for serial interfaces are described in Section 4.1.

8.2 I²C INTERFACE

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ICM-40609-D always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDDIO. The maximum bus speed is 1 MHz.

The slave address of the ICM-40609-D is b110100X, which is 7 bits long. The LSB bit of the 7-bit address is determined by the logic level on pin AP_ADO. This allows two ICM-40609-Ds to be connected to the same I²C bus. When used in this configuration, the address of one of the devices should be b1101000 (pin AP_ADO is logic low) and the address of the other should be b1101001 (pin AP_ADO is logic high).

8.3 I²C COMMUNICATIONS PROTOCOL

START (S) and STOP (P) Conditions

Communication on the I²C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below). Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

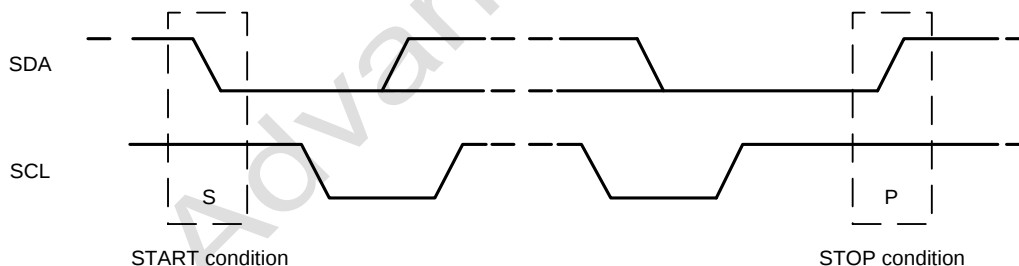


Figure 13. START and STOP Conditions

Data Format / Acknowledge

I²C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).

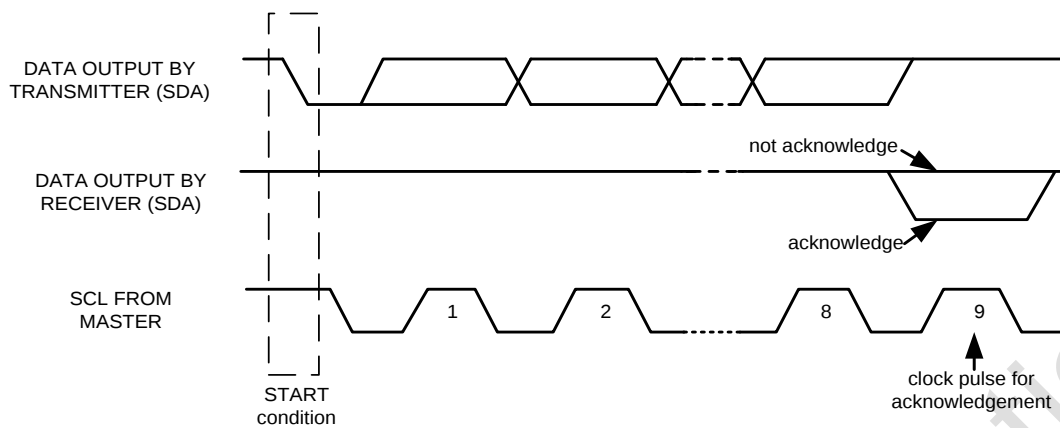


Figure 14. Acknowledge on the I²C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

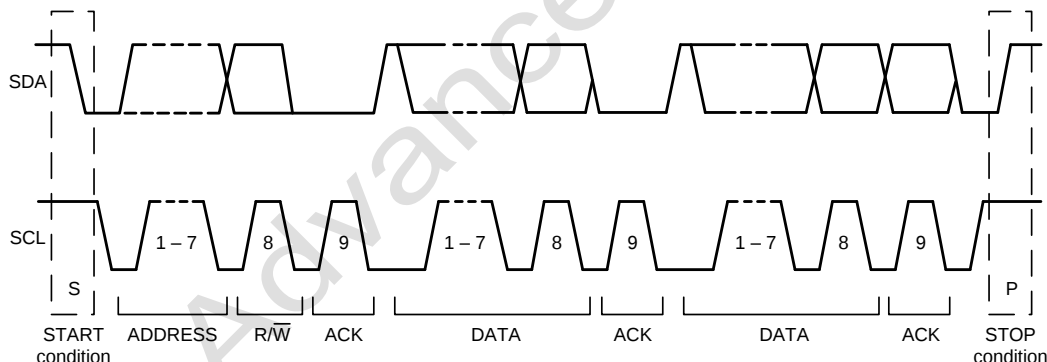


Figure 15. Complete I²C Data Transfer

To write the internal ICM-40609-D registers, the master transmits the start condition (S), followed by the I²C address and the write bit (0). At the 9th clock cycle (when the clock is high), the ICM-40609-D acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the ICM-40609-D acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the ICM-40609-D automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal ICM-40609-D registers, the master sends a start condition, followed by the I²C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the ICM-40609-D, the master transmits a start signal followed by the slave address and read bit. As a result, the ICM-40609-D sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

8.4 I²C TERMS

Signal	Description
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I ² C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9 th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9 th clock cycle
RA	ICM-40609-D internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Table 12. I²C Terms

8.5 SPI INTERFACE

The ICM-40609-D supports 3-wire or 4-wire SPI for the host interface. The ICM-40609-D always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SCLK), the Serial Data Output (SDO), the Serial Data Input (SDI), and the Serial Data IO (SDIO) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on the rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. The maximum frequency of SCLK is 24 MHz
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Read/Writes, data is two or more bytes:

SPI Address format

MSB							LSB
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

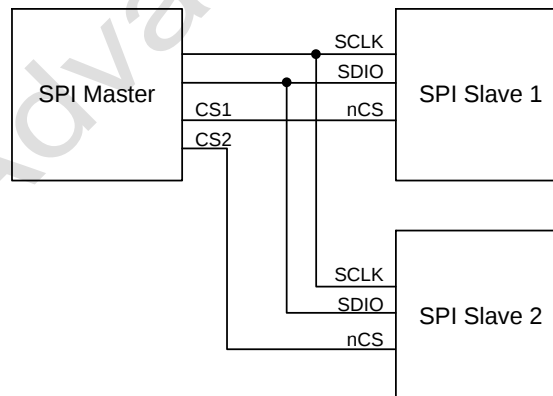


Figure 16. Typical SPI Master/Slave Configuration

9 ASSEMBLY

This section provides general guidelines for assembling InvenSense Micro Electro-Mechanical Systems (MEMS) gyros packaged in LGA package.

9.1 ORIENTATION OF AXES

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

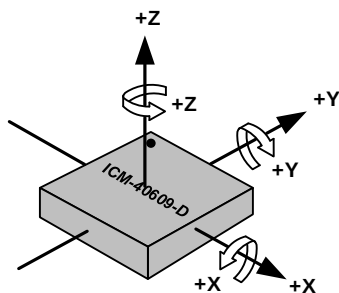
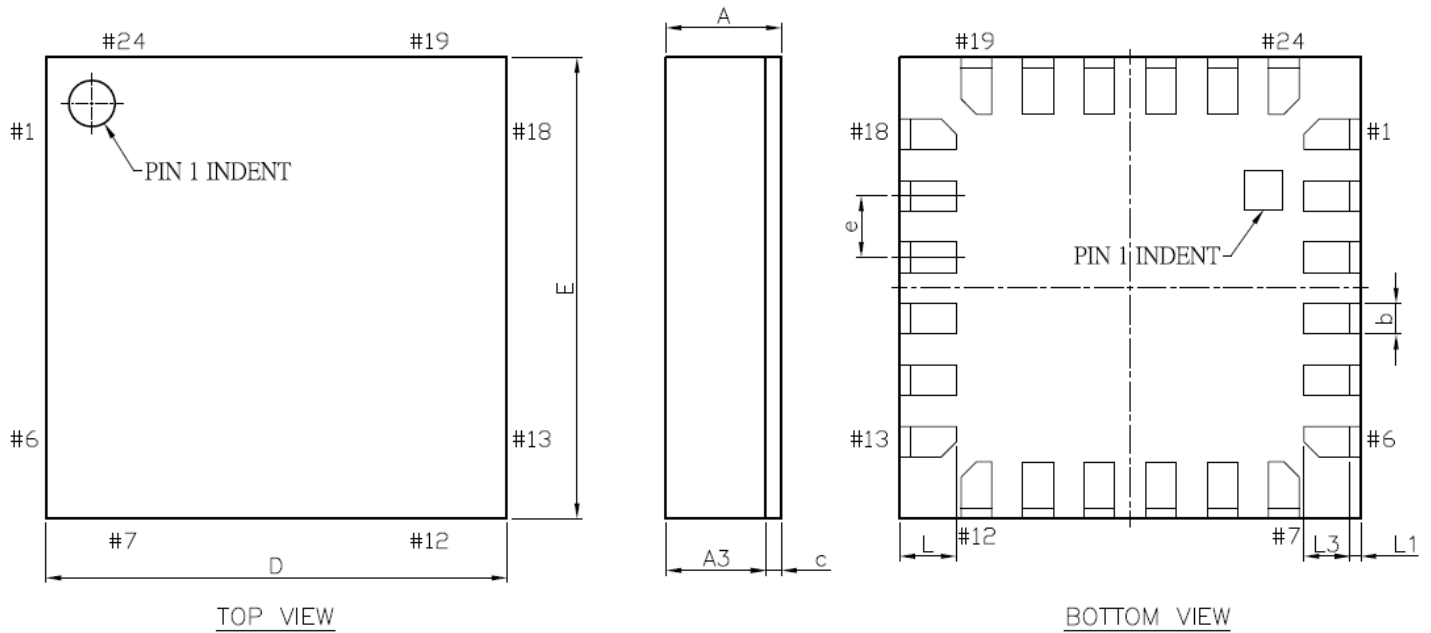


Figure 17. Orientation of Axes of Sensitivity and Polarity of Rotation

9.2 PACKAGE DIMENSIONS

24 Lead LGA (3x3x0.91) mm NiAu pad finish

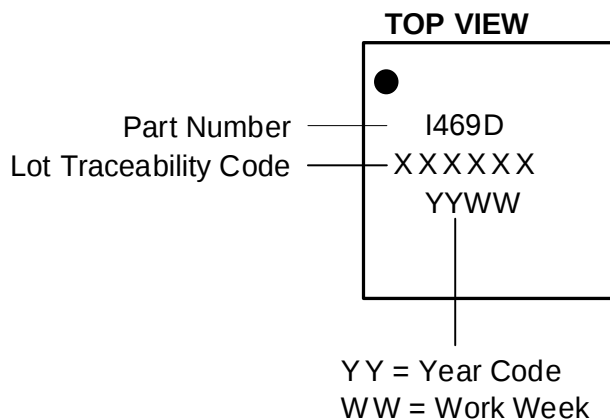


SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.85	0.91	0.97
A3	---	0.8 REF	---
b	0.15	0.20	0.25
c	---	0.105 REF	---
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	---	0.40	---
L	0.32	0.37	0.42
L1	0.02	0.07	0.12
L3	0.25	0.30	0.35
y	0.00	---	0.08

10 PART NUMBER PACKAGE MARKING

The part number package marking for ICM-40609-D devices is summarized below:

Part Number	Part Number Package Marking
ICM-40609-D	I469D



11 CHIP TRACKING METHODOLOGY

This section describes the procedure for retrieval of chip ID information to provide chip tracking capability for the end customer.

The chip ID information is stored in an OTP bank at the time of manufacturing. It consists of 15-bit DieID, 5-bit WaferID, and 36-bit LotID. The IDs can be read using the following command sequence:

1. Write 0x00 to register 0x76 which is accessible from all register banks, to select register bank 0
2. Write 0x10 to register 0x4E, to set the device in IDLE mode
3. Write 0x04 to register 0x71, to enable OTP access
4. Write 0x01 to register 0x76, to select register bank 1
5. Write the following sequence for unlocking OTP reads
 - a. Write 0x18 to register 0x72
 - b. Write 0x06 to register 0x73
 - c. Write 0x00 to register 0x74
6. Write 0x13 to register 0x72, for OTP bank address selection
7. Perform the following sequence to read DieID
 - a. Write 0xDC to register 0x73
 - b. Read register 0x74, it will contain the lower 8 bits of DieID as shown below

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DieID[7]	DieID[6]	DieID[5]	DieID[4]	DieID[3]	DieID[2]	DieID[1]	DieID[0]

- c. Write 0xDD to register 0x73
- d. Read register 0x74, it will contain the upper 7 bits of the DieID as shown below

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ignore	DieID[14]	DieID[13]	DieID[12]	DieID[11]	DieID[10]	DieID[9]	DieID[8]

8. Perform the following sequence to read WaferID
 - a. Write 0xE2 to register 0x73
 - b. Read register 0x74, it will contain the lower 4 bits of WaferID as shown below

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WaferID[3]	WaferID[2]	WaferID[1]	WaferID[0]	Ignore	Ignore	Ignore	Ignore

- c. Write 0xE3 to register 0x73
- d. Read register 0x74, it will contain the upper 1 bit of WaferID as shown below

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ignore	Ignore	Ignore	Ignore	Ignore	Ignore	Ignore	WaferID[4]

9. Perform the following sequence to read LotID

- a. Write 0xDE to register 0x73
- b. Read register 0x74, it will contain part of the LotID as shown below

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LotID_Char2[1]	LotID_Char2[0]	LotID_Char1[5]	LotID_Char1[4]	LotID_Char1[3]	LotID_Char1[2]	LotID_Char1[1]	LotID_Char1[0]

- c. Write 0xDF to register 0x73
- d. Read register 0x74, it will contain part of the LotID as shown below

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-------	-------	-------	-------	-------	-------	-------	-------

LotID_Char3[3]	LotID_Char3[2]	LotID_Char3[1]	LotID_Char3[0]	LotID_Char2[5]	LotID_Char2[4]	LotID_Char2[3]	LotID_Char2[2]
----------------	----------------	----------------	----------------	----------------	----------------	----------------	----------------

- e. Write 0xE0 to register 0x73
- f. Read register 0x74, it will contain part of the LotID as shown below

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LotID_Char4[5]	LotID_Char4[4]	LotID_Char4[3]	LotID_Char4[2]	LotID_Char4[1]	LotID_Char4[0]	LotID_Char3[5]	LotID_Char3[4]

- g. Write 0xE1 to register 0x73
- h. Read register 0x74, it will contain part of the LotID as shown below

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LotID_Char6[1]	LotID_Char6[0]	LotID_Char5[5]	LotID_Char5[4]	LotID_Char5[3]	LotID_Char5[2]	LotID_Char5[1]	LotID_Char5[0]

- i. Write 0xE2 to register 0x73
- j. Read register 0x74, it will contain part of the LotID as shown below

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ignore	Ignore	Ignore	Ignore	LotID_Char6[5]	LotID_Char6[4]	LotID_Char6[3]	LotID_Char6[2]

10. Complete OTP access using the following sequence

- a. Write 0x18 to register 0x72
- b. Write 0x06 to register 0x73
- c. Write 0x06 to register 0x74
- d. Write 0x00 to register 0x76

11. Write 0x00 to register 0x71 to disable OTP access

12. Write 0x00 to register 0x4E to reset/re-start the device

12 USE NOTES

12.1 ACCELEROMETER MODE TRANSITIONS

When transitioning from accelerometer Low Power (LP) mode to accelerometer Low Noise (LN) mode, if ODR is 6.25Hz or lower, software should change ODR to a value of 12.5Hz or higher, because accelerometer LN mode does not support ODR values below 12.5Hz.

When transitioning from accelerometer LN mode to accelerometer LP mode, if ODR is greater than 500Hz, software should change ODR to a value of 500Hz or lower, because accelerometer LP mode does not support ODR values above 500Hz.

12.2 ACCELEROMETER LOW POWER (LP) MODE AVERAGING FILTER SETTING

Software drivers provided with the device use Averaging Filter setting of 16x. This setting is recommended for meeting Android noise requirements in LP mode, and to minimize accelerometer offset variation when transitioning from LP to Low Noise (LN) mode. 1x averaging filter can be used by following the setting configuration shown in section 14.38.

12.3 SETTINGS FOR I²C, AND SPI OPERATION

Upon bootup the device comes up in SPI mode. The following settings should be used for I²C, and SPI operation.

Register Field	I ² C Driver Setting	SPI Driver Setting
I2C_SLEW_RATE (bits 5:3, register DRIVE_CONFIG, address 0x13, bank 0)	1	0
SPI_SLEW_RATE (bits 2:0, register DRIVE_CONFIG, address 0x13, bank 0)	1	5

12.4 NOTCH FILTER AND ANTI-ALIAS FILTER OPERATION

Use of Notch Filter and Anti-Alias Filter is supported only for Low Noise (LN) mode operation. The host is responsible for keeping the UI path in LN mode while Notch Filter and Anti-Alias Filter are turned on.

13 REGISTER MAP

This section lists the register map for the ICM-42605, for user banks 0, 1, 2, 4.

13.1 USER BANK 0 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
11	17	DEVICE_CONFIG	R/W	-			SPI_MODE					SOFT_RESET_CONFIG
13	19	DRIVE_CONFIG	R/W	-		I2C_SLEW_RATE			SPI_SLEW_RATE			
14	20	INT_CONFIG	R/W	-		INT2_MODE	INT2_DRIVE_CIRCUIT	INT2_POLARITY	INT1_MODE	INT1_DRIVE_CIRCUIT	INT1_POLARITY	
16	22	FIFO_CONFIG	R/W	FIFO_MODE		-						
1D	29	TEMP_DATA1	SYNCR	TEMP_DATA[15:8]								
1E	30	TEMP_DATA0	SYNCR	TEMP_DATA[7:0]								
1F	31	ACCEL_DATA_X1	SYNCR	ACCEL_DATA_X[15:8]								
20	32	ACCEL_DATA_X0	SYNCR	ACCEL_DATA_X[7:0]								
21	33	ACCEL_DATA_Y1	SYNCR	ACCEL_DATA_Y[15:8]								
22	34	ACCEL_DATA_Y0	SYNCR	ACCEL_DATA_Y[7:0]								
23	35	ACCEL_DATA_Z1	SYNCR	ACCEL_DATA_Z[15:8]								
24	36	ACCEL_DATA_Z0	SYNCR	ACCEL_DATA_Z[7:0]								
25	37	GYRO_DATA_X1	SYNCR	GYRO_DATA_X[15:8]								
26	38	GYRO_DATA_X0	SYNCR	GYRO_DATA_X[7:0]								
27	39	GYRO_DATA_Y1	SYNCR	GYRO_DATA_Y[15:8]								
28	40	GYRO_DATA_Y0	SYNCR	GYRO_DATA_Y[7:0]								
29	41	GYRO_DATA_Z1	SYNCR	GYRO_DATA_Z[15:8]								
2A	42	GYRO_DATA_Z0	SYNCR	GYRO_DATA_Z[7:0]								
2D	45	INT_STATUS	R/C	-		PLL_RDY_INT	-	DATA_RDY_INT	FIFO_THS_INT	FIFO_FULL_INT	AGC_RDY_INT	
2E	46	FIFO_COUNTH	R	FIFO_COUNT[15:8]								
2F	47	FIFO_COUNTL	R	FIFO_COUNT[7:0]								
30	48	FIFO_DATA	R	FIFO_DATA								
37	55	INT_STATUS2	R/C	-					WOM_Z_INT	WOM_Y_INT	WOM_X_INT	
4B	75	SIGNAL_PATH_RESET	W/C	-					TMST_STROBE	FIFO_FLUSH	-	
4C	76	INTF_CONFIG0	R/W	FIFO_HOLD_LAST_DATA_EN	FIFO_COUNT_REC	FIFO_COUNT_ENDIAN	SENSOR_DATA_ENDIAN	-		UI_SIFS_CFG		
4D	77	INTF_CONFIG1	R/W	-				ACCEL_LP_CLK_SEL	-	CLKSEL		
4E	78	PWR_MGMT0	R/W	-		TEMP_DIS	IDLE	GYRO_MODE		ACCEL_MODE		
4F	79	GYRO_CONFIG0	R/W	GYRO_FS_SEL			-	GYRO_ODR				
50	80	ACCEL_CONFIG0	R/W	ACCEL_FS_SEL			-	ACCEL_ODR				
51	81	GYRO_CONFIG1	R/W	TEMP_FILT_BW			-	GYRO_UI_FILT_ORD		GYRO_DEC2_M2_ORD		
52	82	GYRO_ACCEL_CONFIG0	R/W	ACCEL_UI_FILT_BW			GYRO_UI_FILT_BW					
53	83	ACCEL_CONFIG1	R/W	-			ACCEL_UI_FILT_ORD		ACCEL_DEC2_M2_ORD		-	
54	84	TMST_CONFIG	R/W	-				TMST_RES	TMST_DELTA_EN	-	TMST_EN	
57	87	WOM_CONFIG	R/W	-				WOM_INT_MODE	WOM_MODE	WOM_MODE1		
5F	95	FIFO_CONFIG1	R/W	-	FIFO_RESUME_PARTIAL_READ	FIFO_WM_G_T_TH	-		FIFO_TEMP_EN	FIFO_GYRO_EN	FIFO_ACCEL_EN	
60	96	FIFO_CONFIG2	R/W	FIFO_WM[7:0]								
61	97	FIFO_CONFIG3	R/W	-				FIFO_WM[11:8]				
63	99	INT_CONFIG0	R/W	-		UI_DRDY_INT_CLEAR		FIFO_THS_INT_CLEAR		FIFO_FULL_INT_CLEAR		
65	101	INT_SOURCE0	R/W	-		PLL_RDY_INT1_EN	-	UI_DRDY_INT1_EN	FIFO_THS_INT1_EN	FIFO_FULL_INT1_EN	UI_AGC_RDY_INT1_EN	

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
66	102	INT_SOURCE1	R/W	-					WOM_Z_INT1_EN	WOM_Y_INT1_EN	WOM_X_INT1_EN
68	104	INT_SOURCE3	R/W	-		PLL_RDY_INT2_EN	-	UI_DRDY_INT2_EN	FIFO_THS_INT2_EN	FIFO_FULL_INT2_EN	UI_AGC_RDY_INT2_EN
69	105	INT_SOURCE4	R/W	-					WOM_Z_INT2_EN	WOM_Y_INT2_EN	WOM_X_INT2_EN
6C	108	FIFO_LOST_PKT0	R	FIFO_LOST_PKT_CNT[15:8]							
6D	109	FIFO_LOST_PKT1	R	FIFO_LOST_PKT_CNT[7:0]							
70	112	SELF_TEST_CONFIG	R/W		ACCEL_ST_POWER	EN_AZ_ST	EN_AY_ST	EN_AX_ST	EN_GZ_ST	EN_GY_ST	EN_GX_ST
71	113	OTP_ACCESS	R/W	ENABLE_OTP_ACCESS							
75	117	WHO_AM_I	R	WHOAMI							
76	118	REG_BANK_SEL	R/W	-					BANK_SEL		

13.2 USER BANK 1 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
03	03	SENSOR_CONFIG0	R/W	-		ZG_DISABLE	YG_DISABLE	XG_DISABLE	ZA_DISABLE	YA_DISABLE	XA_DISABLE	
0B	11	GYRO_CONFIG_STATIC2	R/W	-						GYRO_AAF_DIS	GYRO_NF_DIS	
0C	12	GYRO_CONFIG_STATIC3	R/W	-		GYRO_AAF_DELT						
0D	13	GYRO_CONFIG_STATIC4	R/W	GYRO_AAF_DELTSQR[7:0]								
0E	14	GYRO_CONFIG_STATIC5	R/W	GYRO_AAF_BITSHIFT				GYRO_AAF_DELTSQR[11:8]				
0F	15	GYRO_CONFIG_STATIC6	R/W	GYRO_X_NF_COSWZ[7:0]								
10	16	GYRO_CONFIG_STATIC7	R/W	GYRO_Y_NF_COSWZ[7:0]								
11	17	GYRO_CONFIG_STATIC8	R/W	GYRO_Z_NF_COSWZ[7:0]								
12	18	GYRO_CONFIG_STATIC9	R/W	-		GYRO_Z_NF_COSWZ_SEL[0]	GYRO_Y_NF_COSWZ_SEL[0]	GYRO_X_NF_COSWZ_SEL[0]	GYRO_Z_NF_COSWZ[8]	GYRO_Y_NF_COSWZ[8]	GYRO_X_NF_COSWZ[8]	
13	19	GYRO_CONFIG_STATIC10	R/W	-	GYRO_NF_BW_SEL			GYRO_HPF_BW_IND			GYRO_HPF_ORD_IND	
5F	95	XG_ST_DATA	R/W	XG_ST_DATA								
60	96	YG_ST_DATA	R/W	YG_ST_DATA								
61	97	ZG_ST_DATA	R/W	ZG_ST_DATA								
62	98	TMSTVAL0	R	TMST_VALUE[7:0]								
63	99	TMSTVAL1	R	TMST_VALUE[15:8]								
64	100	TMSTVAL2	R	-				TMST_VALUE[19:16]				
72	114	OTP_MEM_BANK_SEL	R/W	OTP_BANK_SEL								
73	115	OTP_MEM_START_ADDR	R/W	OTP_START_ADDR								
74	116	OTP_MEM_READ_WRITE	R/W	OT_READ_WRITE								
7A	122	INTF_CONFIG4	R/W	-						SPI_AP_4WIRE		-
7B	123	INTF_CONFIG5	R/W	-					PIN9_FUNCTION		-	

13.3 USER BANK 2 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
03	03	ACCEL_CONFIG_STATIC2	R/W	-	ACCEL_AAF_DELT						ACCEL_AAF_DIS
04	04	ACCEL_CONFIG_STATIC3	R/W	ACCEL_AAF_DELTSQR[7:0]							
05	05	ACCEL_CONFIG_STATIC4	R/W	ACCEL_AAF_BITSHIFT				ACCEL_AAF_DELTSQR[11:8]			
3B	59	XA_ST_DATA	R/W	XA_ST_DATA							
3C	60	YA_ST_DATA	R/W	YA_ST_DATA							
3D	61	ZA_ST_DATA	R/W	ZA_ST_DATA							

13.4 USER BANK 4 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4A	74	ACCEL_WOM_X_THR	R/W	WOM_X_TH							
4B	75	ACCEL_WOM_Y_THR	R/W	WOM_Y_TH							
4C	76	ACCEL_WOM_Z_THR	R/W	WOM_Z_TH							
77	119	OFFSET_USER0	R/W	GYRO_X_OFFUSER[7:0]							
78	120	OFFSET_USER1	R/W	GYRO_Y_OFFUSER[11:8]				GYRO_X_OFFUSER[11:8]			
79	121	OFFSET_USER2	R/W	GYRO_Y_OFFUSER[7:0]							
7A	122	OFFSET_USER3	R/W	GYRO_Z_OFFUSER[7:0]							
7B	123	OFFSET_USER4	R/W	ACCEL_X_OFFUSER[11:8]				GYRO_Z_OFFUSER[11:8]			
7C	124	OFFSET_USER5	R/W	ACCEL_X_OFFUSER[7:0]							
7D	125	OFFSET_USER6	R/W	ACCEL_Y_OFFUSER[7:0]							
7E	126	OFFSET_USER7	R/W	ACCEL_Z_OFFUSER[11:8]				ACCEL_Y_OFFUSER[11:8]			
7F	127	OFFSET_USER8	R/W	ACCEL_Z_OFFUSER[7:0]							

Detailed register descriptions are provided in the sections that follow. Please note the following regarding Clock Domain for each register:

1. Clock Domain: SCLK_UI means that the register is controlled from the UI interface

14 USER BANK 0 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within USR Bank 0.

Note: The device powers up in sleep mode.

14.1 DEVICE_CONFIG

Name: DEVICE_CONFIG Address: 17 (11h) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:5	-	Reserved
4:1	SPI_MODE	SPI mode selection 0000: Mode 0 and Mode 3 (default) 0001: Mode 1 and Mode 2 Rest of the values are reserved
0	SOFT_RESET_CONFIG	Software reset configuration 0: Normal (default) 1: Enable reset

14.2 DRIVE_CONFIG

Name: DRIVE_CONFIG Address: 19 (13h) Serial IF: R/W Reset value: 0x05 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:6	-	Reserved
5:3	I2C_SLEW_RATE	Controls slew rate for output pin 14 in I ² C mode only 000: 20ns-60ns 001: 12ns-36ns 010: 6ns-18ns 011: 4ns-12ns 100: 2ns-6ns 101: < 2ns 110: Reserved 111: Reserved
2:0	SPI_SLEW_RATE	Controls slew rate for output pin 14 in SPI mode, and for all other output pins 000: 20ns-60ns 001: 12ns-36ns 010: 6ns-18ns 011: 4ns-12ns 100: 2ns-6ns 101: < 2ns 110: Reserved 111: Reserved

14.3 INT_CONFIG

Name: INT_CONFIG Address: 20 (14h) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_OIS1		
BIT	NAME	FUNCTION
7:6	-	Reserved
5	INT2_MODE	INT2 interrupt mode 0: Pulsed mode 1: Latched mode
4	INT2_DRIVE_CIRCUIT	INT2 drive circuit 0: Open drain 1: Push pull
3	INT2_POLARITY	INT2 interrupt polarity 0: Active low (default) 1: Active high
2	INT1_MODE	INT1 interrupt mode 0: Pulsed mode 1: Latched mode
1	INT1_DRIVE_CIRCUIT	INT1 drive circuit 0: Open drain 1: Push pull
0	INT1_POLARITY	INT1 interrupt polarity 0: Active low (default) 1: Active high

14.4 FIFO_CONFIG

Name: FIFO_CONFIG Address: 22 (16h) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:6	FIFO_MODE	00: Bypass Mode (default) 01: Stream-to-FIFO Mode 10: STOP-on-FULL Mode 11: STOP-on-FULL Mode
5:0	-	Reserved

14.5 TEMP_DATA1

Name: TEMP_DATA1 Address: 29 (1Dh) Serial IF: SYNCR Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	TEMP_DATA[15:8]	Upper byte of temperature data

14.6 TEMP_DATA0

Name: TEMP_DATA0		
Address: 30 (1Eh)		
Serial IF: SYNCR		
Reset value: 0x00		
Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	TEMP_DATA[7:0]	Lower byte of temperature data

Temperature data value from the sensor data registers can be converted to degrees centigrade by using the following formula:

$$\text{Temperature in Degrees Centigrade} = (\text{TEMP_DATA} / 132.48) + 25$$

Temperature data stored in FIFO is an 8-bit quantity, FIFO_TEMP_DATA. It can be converted to degrees centigrade by using the following formula:

$$\text{Temperature in Degrees Centigrade} = (\text{FIFO_TEMP_DATA} / 2.07) + 25$$

14.7 ACCEL_DATA_X1

Name: ACCEL_DATA_X1		
Address: 31 (1Fh)		
Serial IF: SYNCR		
Reset value: 0x00		
Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	ACCEL_DATA_X[15:8]	Upper byte of Accel X-axis data

14.8 ACCEL_DATA_X0

Name: ACCEL_DATA_X0		
Address: 32 (20h)		
Serial IF: SYNCR		
Reset value: 0x00		
Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	ACCEL_DATA_X[7:0]	Lower byte of Accel X-axis data

14.9 ACCEL_DATA_Y1

Name: ACCEL_DATA_Y1		
Address: 33 (21h)		
Serial IF: SYNCR		
Reset value: 0x00		
Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Y[15:8]	Upper byte of Accel Y-axis data

14.10 ACCEL_DATA_Y0

Name: ACCEL_DATA_Y0 Address: 34 (22h) Serial IF: SYNCR Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Y[7:0]	Lower byte of Accel Y-axis data

14.11 ACCEL_DATA_Z1

Name: ACCEL_DATA_Z1 Address: 35 (23h) Serial IF: SYNCR Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Z[15:8]	Upper byte of Accel Z-axis data

14.12 ACCEL_DATA_Z0

Name: ACCEL_DATA_Z0 Address: 36 (24h) Serial IF: SYNCR Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Z[7:0]	Lower byte of Accel Z-axis data

14.13 GYRO_DATA_X1

Name: GYRO_DATA_X1 Address: 37 (25h) Serial IF: SYNCR Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	GYRO_DATA_X[15:8]	Upper byte of Gyro X-axis data

14.14 GYRO_DATA_X0

Name: GYRO_DATA_X0 Address: 38 (26h) Serial IF: SYNCR Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	GYRO_DATA_X[7:0]	Lower byte of Gyro X-axis data

14.15 GYRO_DATA_Y1

Name: GYRO_DATA_Y1
Address: 39 (27h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	GYRO_DATA_Y[15:8]	Upper byte of Gyro Y-axis data

14.16 GYRO_DATA_Y0

Name: GYRO_DATA_Y0
Address: 40 (28h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	GYRO_DATA_Y[7:0]	Lower byte of Gyro Y-axis data

14.17 GYRO_DATA_Z1

Name: GYRO_DATA_Z1
Address: 41 (29h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	GYRO_DATA_Z[15:8]	Upper byte of Gyro Z-axis data

14.18 GYRO_DATA_Z0

Name: GYRO_DATA_Z0
Address: 42 (2Ah)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	GYRO_DATA_Z[7:0]	Lower byte of Gyro Z-axis data

14.19 INT_STATUS

Name: INT_STATUS Address: 45 (2Dh) Serial IF: R/C Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:6	-	Reserved
5	PLL_RDY_INT	This bit automatically sets to 1 when a PLL Ready interrupt is generated. The bit clears to 0 after the register has been read.
4	-	Reserved
3	DATA_RDY_INT	This bit automatically sets to 1 when a Data Ready interrupt is generated. The bit clears to 0 after the register has been read.
2	FIFO_THS_INT	This bit automatically sets to 1 when the FIFO buffer reaches the threshold value. The bit clears to 0 after the register has been read.
1	FIFO_FULL_INT	This bit automatically sets to 1 when the FIFO buffer is full. The bit clears to 0 after the register has been read.
0	AGC_RDY_INT	This bit automatically sets to 1 when an AGC Ready interrupt is generated. The bit clears to 0 after the register has been read.

14.20 FIFO_COUNTH

Name: FIFO_COUNTH Address: 46 (2Eh) Serial IF: R Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	FIFO_COUNT[15:8]	High Bits, count indicates the number of records or bytes available in FIFO according to FIFO_COUNT_REC setting. Note: Must read FIFO_COUNTL to latch new data for both FIFO_COUNTH and FIFO_COUNTL.

14.21 FIFO_COUNTL

Name: FIFO_COUNTL Address: 47 (2Fh) Serial IF: R Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	FIFO_COUNT[7:0]	Low Bits, count indicates the number of records or bytes available in FIFO according to FIFO_COUNT_REC setting. Reading this byte latches the data for both FIFO_COUNTH, and FIFO_COUNTL.

14.22 FIFO_DATA

Name: FIFO_DATA		
Address: 48 (30h)		
Serial IF: R		
Reset value: 0xFF		
Clock Domain: SCLK_UI		
BITS	NAME	FUNCTION
7:0	FIFO_DATA	FIFO data port

14.23 INT_STATUS2

Name: INT_STATUS2		
Address: 55 (37h)		
Serial IF: R/C		
Reset value: 0x00		
Clock Domain: SCLK_UI		
BITS	NAME	FUNCTION
7:3	-	Reserved
2	WOM_Z_INT	Wake on Motion Interrupt on Z-axis, clears on read
1	WOM_Y_INT	Wake on Motion Interrupt on Y-axis, clears on read
0	WOM_X_INT	Wake on Motion Interrupt on X-axis, clears on read

14.24 SIGNAL_PATH_RESET

Name: SIGNAL_PATH_RESET		
Address: 75 (4Bh)		
Serial IF: W/C		
Reset value: 0x00		
Clock Domain: SCLK_UI		
BITS	NAME	FUNCTION
7:3	-	Reserved
2	TMST_STROBE	When this bit is set to 1, the time stamp counter is latched into the time stamp register. This is a write on clear bit.
1	FIFO_FLUSH	When set to 1, FIFO will get flushed.
0	-	Reserved

14.25 INTF_CONFIG0

Name: INTF_CONFIG0 Address: 76 (4Ch) Serial IF: R/W Reset value: 0x30 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7	FIFO_HOLD_LAST_DATA_EN	0: If Accel and Gyro ODRs are different, decimal value -32768 will be written to FIFO for the sensor with lower ODR until new sensor data is available. If Accel or Gyro ODR is > 8kHz, Temp sensor ODR will be limited to 8kHz and decimal value -128 will be written to FIFO until new sensor data is available. 1: If Accel, and Gyro ODRs are different, last valid data is rewritten to FIFO for the sensor with lower ODR until new sensor data is available. If Accel or Gyro ODR is > 8kHz, Temp sensor data will be limited to 8kHz and last valid data for Temp sensor will be rewritten to FIFO until new sensor data is available.
6	FIFO_COUNT_REC	0: FIFO count is reported in bytes 1: FIFO count is reported in records (1 record = 16 bytes for header + gyro + accel + temp sensor data + time stamp, or 8 bytes for header + gyro/accel + temp sensor data)
5	FIFO_COUNT_ENDIAN	0: FIFO count is reported in Little Endian format 1: FIFO count is reported in Big Endian format (default)
4	SENSOR_DATA_ENDIAN	0: Sensor data is reported in Little Endian format 1: Sensor data is reported in Big Endian format (default)
3:2	-	Reserved
1:0	UI_SIFS_CFG	0x: Reserved 10: Disable SPI 11: Disable I2C

14.26 INTF_CONFIG1

Name: INTF_CONFIG1 Address: 77 (4Dh) Serial IF: R/W Reset value: 0x51 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:4	-	Reserved
3	ACCEL_LP_CLK_SEL	0: Accelerometer LP mode uses Wake Up oscillator clock (default) 1: Reserved
2	-	Reserved
1:0	CLKSEL	00: Always select internal RC oscillator 01: Select PLL when available, else select RC oscillator (default) 10: Reserved 11: Disable all clocks

14.27 PWR_MGMT0

Name: PWR_MGMT0 Address: 78 (4Eh) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:6	-	Reserved
5	TEMP_DIS	0: Temperature sensor is enabled (default) 1: Temperature sensor is disabled
4	IDLE	If this bit is set to 1, the RC oscillator is powered on even if Accel and Gyro are powered off. Nominally this bit is set to 0, so when Accel and Gyro are powered off, the chip will go to OFF state, since the RC oscillator will also be powered off
3:2	GYRO_MODE	00: Turns gyroscope off (default) 01: Places gyroscope in Standby Mode 10: Reserved 11: Places gyroscope in Low Noise (LN) Mode Gyroscope needs to be kept ON for a minimum of 45ms. When transitioning from OFF to any of the other modes, do not issue any register writes for 200μs.
1:0	ACCEL_MODE	00: Turns accelerometer off (default) 01: Turns accelerometer off 10: Places accelerometer in Low Power (LP) Mode 11: Places accelerometer in Low Noise (LN) Mode When transitioning from OFF to any of the other modes, do not issue any register writes for 200μs.

14.28 GYRO_CONFIG0

Name: GYRO_CONFIG0

Address: 79 (4Fh)

Serial IF: R/W

Reset value: 0x07

Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:5	GYRO_FS_SEL	Full scale select for gyroscope UI interface output 000: ± 2000 dps (default) 001: ± 1000 dps 010: ± 500 dps 011: ± 250 dps 100: ± 125 dps 101: ± 62.5 dps 110: ± 31.25 dps 111: ± 15.625 dps
4	-	Reserved
3:0	GYRO_ODR	Gyroscope ODR selection for UI interface output 0000: Reserved 0001: 32kHz 0010: 16kHz 0011: 8kHz 0100: 4kHz 0101: 2kHz 0110: 1kHz (default) 0111: 200Hz 1000: 100Hz 1001: 50Hz 1010: 25Hz 1011: 12.5Hz 1100: Reserved 1101: Reserved 1110: Reserved 1111: 500Hz

14.29 ACCEL_CONFIG0

Name: ACCEL_CONFIG0

Address: 80 (50h)

Serial IF: R/W

Reset value: 0x07

Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:5	ACCEL_FS_SEL	Full scale select for accelerometer UI interface output 000: $\pm 32g$ (default) 001: $\pm 16g$ 010: $\pm 8g$ 011: $\pm 4g$ 100: Reserved 101: Reserved 110: Reserved 111: Reserved
4	-	Reserved
3:0	ACCEL_ODR	Accelerometer ODR selection for UI interface output 0000: Reserved 0001: 32kHz (LN mode) 0010: 16kHz (LN mode) 0011: 8kHz (LN mode) 0100: 4kHz (LN mode) 0101: 2kHz (LN mode) 0110: 1kHz (LN mode) (default) 0111: 200Hz (LP or LN mode) 1000: 100Hz (LP or LN mode) 1001: 50Hz (LP or LN mode) 1010: 25Hz (LP or LN mode) 1011: 12.5Hz (LP or LN mode) 1100: 6.25Hz (LP mode) 1101: 3.125Hz (LP mode) 1110: 1.5625Hz (LP mode) 1111: 500Hz (LP or LN mode)

14.30 GYRO_CONFIG1

Name: GYRO_CONFIG1
 Address: 81 (51h)
 Serial IF: R/W
 Reset value: 0x1A
 Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:5	TEMP_FILT_BW	Sets the bandwidth of the temperature signal DLPF 000: DLPF BW = 4000Hz; DLPF Latency = 0.125ms (default) 001: DLPF BW = 170Hz; DLPF Latency = 1ms 010: DLPF BW = 82Hz; DLPF Latency = 2ms 011: DLPF BW = 40Hz; DLPF Latency = 4ms 100: DLPF BW = 20Hz; DLPF Latency = 8ms 101: DLPF BW = 10Hz; DLPF Latency = 16ms 110: DLPF BW = 5Hz; DLPF Latency = 32ms 111: DLPF BW = 5Hz; DLPF Latency = 32ms
4	-	Reserved
3:2	GYRO_UI_FILT_ORD	Selects order of GYRO UI FIR filter 00: 1 st Order 01: 2 nd Order 10: 3 rd Order 11: Reserved
1:0	GYRO_DEC2_M2_ORD	Selects order of GYRO DEC2_M2 Filter 00: 1 st Order 01: 2 nd Order 10: 3 rd Order 11: Reserved

14.31 GYRO_ACCEL_CONFIG0

Name: GYRO_ACCEL_CONFIG0

Address: 82 (52h)

Serial IF: R/W

Reset value: 0x11

Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:4	ACCEL_UI_FILT_BW	LN Mode: Bandwidth for Accel LPF 0 BW=ODR/2 1 BW=max(400Hz, ODR)/4 (default) 2 BW=max(400Hz, ODR)/5 3 BW=max(400Hz, ODR)/8 4 BW=max(400Hz, ODR)/10 5 BW=max(400Hz, ODR)/16 6 BW=max(400Hz, ODR)/20 7 BW=max(400Hz, ODR)/40 8 to 13: Reserved 14 Low Latency option: Trivial decimation @ ODR of Dec2 filter output. Dec2 runs at max(400Hz, ODR) 15 Low Latency option: Trivial decimation @ ODR of Dec2 filter output. Dec2 runs at max(200Hz, 8*ODR) LP Mode: 0 Reserved 1 1x AVG filter (default) 2 to 5 Reserved 6 16x AVG filter 7 to 15 Reserved
3:0	GYRO_UI_FILT_BW	LN Mode: Bandwidth for Gyro LPF 0 BW=ODR/2 1 BW=max(400Hz, ODR)/4 (default) 2 BW=max(400Hz, ODR)/5 3 BW=max(400Hz, ODR)/8 4 BW=max(400Hz, ODR)/10 5 BW=max(400Hz, ODR)/16 6 BW=max(400Hz, ODR)/20 7 BW=max(400Hz, ODR)/40 8 to 13: Reserved 14 Low Latency option: Trivial decimation @ ODR of Dec2 filter output. Dec2 runs at max(400Hz, ODR) 15 Low Latency option: Trivial decimation @ ODR of Dec2 filter output. Dec2 runs at max(200Hz, 8*ODR)

14.32 ACCEL_CONFIG1

Name: ACCEL_CONFIG1 Address: 83 (53h) Serial IF: R/W Reset value: 0x15 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:5	-	Reserved
4:3	ACCEL_UI_FILT_ORD	Selects order of ACCEL UI FIR filter 00: 1 st Order 01: 2 nd Order 10: 3 rd Order 11: Reserved
2:1	ACCEL_DEC2_M2_ORD	Order of Accelerometer DEC2_M2 filter 00: 1 st order 01: 2 nd order 10: 3 rd order 11: Reserved
0	-	Reserved

14.33 TMST_CONFIG

Name: TMST_CONFIG Address: 84 (54h) Serial IF: R/W Reset value: 0x20 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:4	-	Reserved
3	TMST_RES	Time Stamp resolution: When set to 0 (default), time stamp resolution is 1 μ s. When set to 1, resolution is 16 μ s
2	TMST_DELTA_EN	Time Stamp delta enable: When set to 1, the time stamp field contains the measurement of time since the last occurrence of ODR.
1	-	Reserved
0	TMST_EN	0: Time Stamp register disable 1: Time Stamp register enable (default)

14.34 WOM_CONFIG

Name: WOM_CONFIG Address: 87 (57h) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:4	-	Reserved
3	WOM_INT_MODE	0: Set WoM interrupt on the OR of all enabled accelerometer thresholds 1: Set WoM interrupt on the AND of all enabled accelerometer threshold
2	WOM_MODE	0: Initial sample is stored. Future samples are compared to initial sample 1: Compare current sample to previous sample
1:0	WOM_MODE1	00: Reserved 01: Set to 1 for WOM interrupt configuration 10: Reserved 11: Reserved

14.35 FIFO_CONFIG1

Name: FIFO_CONFIG1 Address: 95 (5Fh) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7	-	Reserved
6	FIFO_RESUME_PARTIAL_RD	0: Partial FIFO read disabled, requires re-reading of the entire FIFO 1: FIFO read can be partial, and resume from last read point
5	FIFO_WM_GT_TH	Trigger FIFO watermark interrupt on every ODR (DMA write) if $FIFO_COUNT \geq FIFO_WM_TH$
4:3	-	Reserved
2	FIFO_TEMP_EN	Enable temperature sensor packets to go to FIFO
1	FIFO_GYRO_EN	Enable gyroscope packets to go to FIFO
0	FIFO_ACCEL_EN	Enable accelerometer packets to go to FIFO

14.36 FIFO_CONFIG2

Name: FIFO_CONFIG2 Address: 96 (60h) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	FIFO_WM[7:0]	Lower bits of FIFO watermark. Generate interrupt when the FIFO reaches or exceeds FIFO_WM size in bytes or records according to FIFO_COUNT_REC setting. FIFO_WM_EN must be zero before writing this register. Interrupt only fires once. This register should be set to non-zero value, before choosing this interrupt source.

14.37 FIFO_CONFIG3

Name: FIFO_CONFIG3 Address: 97 (61h) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:4	-	Reserved
3:0	FIFO_WM[11:8]	Upper bits of FIFO watermark. Generate interrupt when the FIFO reaches or exceeds FIFO_WM size in bytes or records according to FIFO_COUNT_REC setting. FIFO_WM_EN must be zero before writing this register. Interrupt only fires once. This register should be set to non-zero value, before choosing this interrupt source.

Note: Do not set FIFO_WM to value 0.

14.38 INT_CONFIG0

Name: INT_CONFIG0 Address: 99 (63h) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:6	-	Reserved
5:4	UI_DRDY_INT_CLEAR	Data Ready Interrupt Clear Option (latched mode) 00: Clear on Status Bit Read (default) 01: Clear on Status Bit Read 10: Clear on FIFO data 1Byte Read 11: Clear on Status Bit Read AND on FIFO data 1 byte read
3:2	FIFO_THS_INT_CLEAR	FIFO Threshold Interrupt Clear Option (latched mode) 00: Clear on Status Bit Read (default) 01: Clear on Status Bit Read 10: Clear on FIFO data 1Byte Read 11: Clear on Status Bit Read AND on FIFO data 1 byte read
1:0	FIFO_FULL_INT_CLEAR	FIFO Full Interrupt Clear Option (latched mode) 00: Clear on Status Bit Read (default) 01: Clear on Status Bit Read 10: Clear on FIFO data 1Byte Read 11: Clear on Status Bit Read AND on FIFO data 1 byte read

14.39 INT_SOURCE0

Name: INT_SOURCE0		
Address: 101 (65h)		
Serial IF: R/W		
Reset value: 0x10		
Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:6	-	Reserved
5	PLL_RDY_INT1_EN	0: PLL ready interrupt not routed to INT1 1: PLL ready interrupt routed to INT1
4	-	Reserved
3	UI_DRDY_INT1_EN	0: UI data ready interrupt not routed to INT1 1: UI data ready interrupt routed to INT1
2	FIFO_THS_INT1_EN	0: FIFO threshold interrupt not routed to INT1 1: FIFO threshold interrupt routed to INT1
1	FIFO_FULL_INT1_EN	0: FIFO full interrupt not routed to INT1 1: FIFO full interrupt routed to INT1
0	UI_AGC_RDY_INT1_EN	0: UI AGC ready interrupt not routed to INT1 1: UI AGC ready interrupt routed to INT1

14.40 INT_SOURCE1

Name: INT_SOURCE1		
Address: 102 (66h)		
Serial IF: R/W		
Reset value: 0x00		
Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:3	-	Reserved
2	WOM_Z_INT1_EN	0: Z-axis WOM interrupt not routed to INT1 1: Z-axis WOM interrupt routed to INT1
1	WOM_Y_INT1_EN	0: Y-axis WOM interrupt not routed to INT1 1: Y-axis WOM interrupt routed to INT1
0	WOM_X_INT1_EN	0: X-axis WOM interrupt not routed to INT1 1: X-axis WOM interrupt routed to INT1

14.41 INT_SOURCE3

Name: INT_SOURCE3 Address: 104 (68h) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:6	-	Reserved
5	PLL_RDY_INT2_EN	0: PLL ready interrupt not routed to INT2 1: PLL ready interrupt routed to INT2
4	-	Reserved
3	UI_DRDY_INT2_EN	0: UI data ready interrupt not routed to INT2 1: UI data ready interrupt routed to INT2
2	FIFO_THS_INT2_EN	0: FIFO threshold interrupt not routed to INT2 1: FIFO threshold interrupt routed to INT2
1	FIFO_FULL_INT2_EN	0: FIFO full interrupt not routed to INT2 1: FIFO full interrupt routed to INT2
0	UI_AGC_RDY_INT2_EN	0: UI AGC ready interrupt not routed to INT2 1: UI AGC ready interrupt routed to INT2

14.42 INT_SOURCE4

Name: INT_SOURCE4 Address: 105 (69h) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:3	-	Reserved
2	WOM_Z_INT2_EN	0: Z-axis WOM interrupt not routed to INT2 1: Z-axis WOM interrupt routed to INT2
1	WOM_Y_INT2_EN	0: Y-axis WOM interrupt not routed to INT2 1: Y-axis WOM interrupt routed to INT2
0	WOM_X_INT2_EN	0: X-axis WOM interrupt not routed to INT2 1: X-axis WOM interrupt routed to INT2

14.43 FIFO_LOST_PKT0

Name: FIFO_LOST_PKT0 Address: 108 (6Ch) Serial IF: R Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	FIFO_LOST_PKT_CNT[7:0]	Low byte, number of packets lost in the FIFO

14.44 FIFO_LOST_PKT1

Name: FIFO_LOST_PKT1		
Address: 109 (6Dh)		
Serial IF: R		
Reset value: 0x00		
Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	FIFO_LOST_PKT_CNT[15:8]	High byte, number of packets lost in the FIFO

14.45 SELF_TEST_CONFIG

Name: SELF_TEST_CONFIG		
Address: 112 (70h)		
Serial IF: R/W		
Reset value: 0x00		
Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7	-	Reserved
6	ACCEL_ST_POWER	Set to 1 for accel self-test Otherwise set to 0; Set to 0 after self-test is completed
5	EN_AZ_ST	Enable Z-accel self-test
4	EN_AY_ST	Enable Y-accel self-test
3	EN_AX_ST	Enable X-accel self-test
2	EN_GZ_ST	Enable Z-gyro self-test
1	EN_GY_ST	Enable Y-gyro self-test
0	EN_GX_ST	Enable X-gyro self-test

14.46 OTP_ACCESS

Name: ENABLE_OTP_ACCESS		
Address: 113 (71h)		
Serial IF: R/W		
Reset value: 0x00		
Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	ENABLE_OTP_ACCESS	Write 0x04 to this register to enable OTP access

14.47 WHO_AM_I

Name: WHO_AM_I Address: 117 (75h) Serial IF: R Reset value: 0x3B Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	WHOAMI	Register to indicate to user which device is being accessed

Description:

This register is used to verify the identity of the device. The contents of WHOAMI is an 8-bit device ID. The default value of the register is 0x3B. This is different from the I²C address of the device as seen on the slave I²C controller by the applications processor.

14.48 REG_BANK_SEL

Note: This register is accessible from all register banks

Name: REG_BANK_SEL Address: 118 (76h) Serial IF: R/W Reset value: 0x00 Clock Domain: ALL		
BIT	NAME	FUNCTION
7:3	-	Reserved
2:0	BANK_SEL	Register bank selection 000: Bank 0 (default) 001: Bank 1 010: Bank 2 011: Bank 3 100: Bank 4 101: Reserved 110: Reserved 111: Reserved

15 USER BANK 1 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within USR Bank 1.

15.1 SENSOR_CONFIG0

Name: SENSOR_CONFIG0 Address: 03 (03h) Serial IF: R/W Reset value: 0x40 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:6	-	Reserved
5	ZG_DISABLE	0: Z gyroscope is on 1: Z gyroscope is disabled
4	YG_DISABLE	0: Y gyroscope is on 1: Y gyroscope is disabled
3	XG_DISABLE	0: X gyroscope is on 1: X gyroscope is disabled
2	ZA_DISABLE	0: Z accelerometer is on 1: Z accelerometer is disabled
1	YA_DISABLE	0: Y accelerometer is on 1: Y accelerometer is disabled
0	XA_DISABLE	0: X accelerometer is on 1: X accelerometer is disabled

15.2 GYRO_CONFIG_STATIC2

Name: GYRO_CONFIG_STATIC2 Address: 11 (0Bh) Serial IF: R/W Reset value: 0x03 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:2	-	Reserved
1	GYRO_AAF_DIS	0: Enable Anti-Aliasing/Low Pass Filter 1: Disable Anti-Aliasing/Low Pass Filter (default)
0	GYRO_NF_DIS	0: Enable Notch Filter 1: Disable Notch Filter (default)

15.3 GYRO_CONFIG_STATIC3

Name: GYRO_CONFIG_STATIC3 Address: 12 (0Ch) Serial IF: R/W Reset value: 0x3F Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:6	-	Reserved
5:0	GYRO_AAF_DELT	Controls bandwidth of the gyroscope anti-alias filter See section 5.2 for details

15.4 GYRO_CONFIG_STATIC4

Name: GYRO_CONFIG_STATIC4 Address: 13 (0Dh) Serial IF: R/W Reset value: 0x81 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	GYRO_AAF_DELTSQR[7:0]	Controls bandwidth of the gyroscope anti-alias filter See section 5.2 for details

15.5 GYRO_CONFIG_STATIC5

Name: GYRO_CONFIG_STATIC5 Address: 14 (0Eh) Serial IF: R/W Reset value: 0x3F Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:4	GYRO_AAF_BITSHIFT	Controls bandwidth of the gyroscope anti-alias filter See section 5.2 for details
3:0	GYRO_AAF_DELTSQR[11:8]	Controls bandwidth of the gyroscope anti-alias filter See section 5.2 for details

15.6 GYRO_CONFIG_STATIC6

Name: GYRO_CONFIG_STATIC6 Address: 15 (0Fh) Serial IF: R/W Reset value: 0xEA Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	GYRO_X_NF_COSWZ[7:0]	Used for gyroscope X-axis notch filter frequency selection See section 5.1 for details

15.7 GYRO_CONFIG_STATIC7

Name: GYRO_CONFIG_STATIC7 Address: 16 (10h) Serial IF: R/W Reset value: 0x28 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	GYRO_Y_NF_COSWZ[7:0]	Used for gyroscope Y-axis notch filter frequency selection See section 5.1 for details

15.8 GYRO_CONFIG_STATIC8

Name: GYRO_CONFIG_STATIC8 Address: 17 (11h) Serial IF: R/W Reset value: 0x07 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	GYRO_Z_NF_COSWZ[7:0]	Used for gyroscope Z-axis notch filter frequency selection See section 5.1 for details

15.9 GYRO_CONFIG_STATIC9

Name: GYRO_CONFIG_STATIC9 Address: 18 (12h) Serial IF: R/W Reset value: 0x01 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:6	-	Reserved
5	GYRO_Z_NF_COSWZ_SEL[0]	Used for gyroscope Z-axis notch filter frequency selection See section 5.1 for details
4	GYRO_Y_NF_COSWZ_SEL[0]	Used for gyroscope Y-axis notch filter frequency selection See section 5.1 for details
3	GYRO_X_NF_COSWZ_SEL[0]	Used for gyroscope X-axis notch filter frequency selection See section 5.1 for details
2	GYRO_Z_NF_COSWZ[8]	Used for gyroscope Z-axis notch filter frequency selection See section 5.1 for details
1	GYRO_Y_NF_COSWZ[8]	Used for gyroscope Y-axis notch filter frequency selection See section 5.1 for details
0	GYRO_X_NF_COSWZ[8]	Used for gyroscope X-axis notch filter frequency selection See section 5.1 for details

15.10 GYRO_CONFIG_STATIC10

Name: GYRO_CONFIG_STATIC10 Address: 19 (13h) Serial IF: R/W Reset value: 0x11 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7	-	Reserved
6:4	GYRO_NF_BW_SEL	Selects bandwidth for gyroscope notch filter See section 5.1 for details
3:1	GYRO_HPF_BW_IND	Selects HPF 3dB cutoff frequency bandwidth See section 5.6 for details
0	GYRO_HPF_ORD_IND	Selects HPF filter order (see section 5.6 for details) 0: 1 st order HPF 1: 2 nd order HPF

15.11 XG_ST_DATA

Name: XG_ST_DATA
 Address: 95 (5Fh)
 Serial IF: R/W
 Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)
 Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	XG_ST_DATA	X-gyro self-test data

15.12 YG_ST_DATA

Name: YG_ST_DATA
 Address: 96 (60h)
 Serial IF: R/W
 Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)
 Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	YG_ST_DATA	Y-gyro self-test data

15.13 ZG_ST_DATA

Name: ZG_ST_DATA
 Address: 97 (61h)
 Serial IF: R/W
 Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)
 Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	ZG_ST_DATA	Z-gyro self-test data

15.14 TMSTVAL0

Name: TMSTVAL0
 Address: 98 (62h)
 Serial IF: R
 Reset value: 0x00
 Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	TMST_VALUE[7:0]	When TMST_STROBE is programmed, the current value of the internal counter is latched to this register. Allows the full 20-bit precision of the time stamp to be read back.

15.15 TMSTVAL1

Name: TMSTVAL1 Address: 99 (63h) Serial IF: R Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	TMST_VALUE[15:8]	When TMST_STROBE is programmed, the current value of the internal counter is latched to this register. Allows the full 20-bit precision of the time stamp to be read back.

15.16 TMSTVAL2

Name: TMSTVAL2 Address: 100 (64h) Serial IF: R Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:4	-	Reserved
3:0	TMST_VALUE[19:16]	When TMST_STROBE is programmed, the current value of the internal counter is latched to this register. Allows the full 20-bit precision of the time stamp to be read back.

15.17 OTP_MEM_BANK_SEL

Name: OTP_MEM_BANK_SEL Address: 114 (72h) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	OTP_BANK_SEL	Write values to this register as described in Section 11, for accessing chip ID information

15.18 OTP_MEM_START_ADDR

Name: OTP_MEM_START_ADDR Address: 115 (73h) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	OTP_START_ADDR	Write values to this register as described in Section 11, for accessing chip ID information

15.19 OTP_MEM_READ_WRITE

Name: OTP_MEM_READ_WRITE		
Address: 116 (74h)		
Serial IF: R/W		
Reset value: 0x00		
Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	OTP_READ_WRITE	Read/Write values from this register as described in Section 11, for accessing chip ID information

15.20 INTF_CONFIG4

Name: INTF_CONFIG4		
Address: 122 (7Ah)		
Serial IF: R/W		
Reset value: 0x02		
Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:2	-	Reserved
1	SPI_AP_4WIRE	0: AP interface uses 3-wire SPI mode 1: AP interface uses 4-wire SPI mode (default)
0	-	Reserved

15.21 INTF_CONFIG5

Name: INTF_CONFIG5		
Address: 123 (7Bh)		
Serial IF: R/W		
Reset value: 0x24		
Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:3	-	Reserved
2:1	PIN9_FUNCTION	Selects among the following functionalities for pin 9 00: INT2 01: Reserved 10: Reserved 11: Reserved
0	-	Reserved

16 USER BANK 2 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within USR Bank 2.

16.1 ACCEL_CONFIG_STATIC2

Name: ACCEL_CONFIG_STATIC2 Address: 03 (03h) Serial IF: R/W Reset value: 0x7F Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7	-	Reserved
6:1	ACCEL_AAF_DELT	Controls bandwidth of the accelerometer anti-alias filter See section 5.2 for details
0	ACCEL_AAF_DIS	0: Enable accelerometer anti-aliasing filter 1: Disable accelerometer anti-aliasing filter (default)

16.2 ACCEL_CONFIG_STATIC3

Name: ACCEL_CONFIG_STATIC3 Address: 04 (04h) Serial IF: R/W Reset value: 0x81 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	ACCEL_AAF_DELTSQR[7:0]	Controls bandwidth of the accelerometer anti-alias filter See section 5.2 for details

16.3 ACCEL_CONFIG_STATIC4

Name: ACCEL_CONFIG_STATIC4 Address: 05 (05h) Serial IF: R/W Reset value: 0x3F Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:4	ACCEL_AAF_BITSHIFT	Controls bandwidth of the accelerometer anti-alias filter See section 5.2 for details
3:0	ACCEL_AAF_DELTSQR[11:8]	Controls bandwidth of the accelerometer anti-alias filter See section 5.2 for details

16.4 XA_ST_DATA

Name: XA_ST_DATA Address: 59 (3Bh) Serial IF: R/W Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests) Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	XA_ST_DATA	X-accel self-test data

16.5 YA_ST_DATA

Name: YA_ST_DATA
 Address: 60 (3Ch)
 Serial IF: R/W
 Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)
 Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	YA_ST_DATA	Y-accel self-test data

16.6 ZA_ST_DATA

Name: ZA_ST_DATA
 Address: 61 (3Dh)
 Serial IF: R/W
 Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)
 Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	ZA_ST_DATA	Z-accel self-test data

17 USER BANK 4 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within USR Bank 4.

17.1 ACCEL_WOM_X_THR

Name: ACCEL_WOM_X_THR Address: 74 (4Ah) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	WOM_X_TH	Threshold value for the Wake on Motion Interrupt for X-axis accelerometer WoM thresholds are expressed in fixed “mg” independent of the selected Range [0g : 1g]; Resolution 1g/256≈3.9mg

17.2 ACCEL_WOM_Y_THR

Name: ACCEL_WOM_Y_THR Address: 75 (4Bh) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	WOM_Y_TH	Threshold value for the Wake on Motion Interrupt for Y-axis accelerometer WoM thresholds are expressed in fixed “mg” independent of the selected Range [0g : 1g]; Resolution 1g/256≈3.9mg

17.3 ACCEL_WOM_Z_THR

Name: ACCEL_WOM_Z_THR Address: 76 (4Ch) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	WOM_Z_TH	Threshold value for the Wake on Motion Interrupt for Z-axis accelerometer WoM thresholds are expressed in fixed “mg” independent of the selected Range [0g : 1g]; Resolution 1g/256≈3.9mg

17.4 OFFSET_USER0

Name: OFFSET_USER0 Address: 119 (77h) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	GYRO_X_OFFUSER[7:0]	Lower bits of X-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.

17.5 OFFSET_USER1

Name: OFFSET_USER1 Address: 120 (78h) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:4	GYRO_Y_OFFUSER[11:8]	Upper bits of Y-gyro offset programmed by user. Max value is ± 64 dps, resolution is 1/32 dps.
3:0	GYRO_X_OFFUSER[11:8]	Upper bits of X-gyro offset programmed by user. Max value is ± 64 dps, resolution is 1/32 dps.

17.6 OFFSET_USER2

Name: OFFSET_USER2 Address: 121 (79h) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	GYRO_Y_OFFUSER[7:0]	Lower bits of Y-gyro offset programmed by user. Max value is ± 64 dps, resolution is 1/32 dps.

17.7 OFFSET_USER3

Name: OFFSET_USER3 Address: 122 (7Ah) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	GYRO_Z_OFFUSER[7:0]	Lower bits of Z-gyro offset programmed by user. Max value is ± 64 dps, resolution is 1/32 dps.

17.8 OFFSET_USER4

Name: OFFSET_USER4 Address: 123 (7Bh) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:4	ACCEL_X_OFFUSER[11:8]	Upper bits of X-accel offset programmed by user. Max value is ± 64 dps, resolution is 1/32 dps.
3:0	GYRO_Z_OFFUSER[11:8]	Upper bits of Z-gyro offset programmed by user. Max value is ± 64 dps, resolution is 1/32 dps.

17.9 OFFSET_USER5

Name: OFFSET_USER5 Address: 124 (7Ch) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	ACCEL_X_OFFUSER[7:0]	Lower bits of X-accel offset programmed by user. Max value is ± 64 dps, resolution is 1/32 dps.

17.10 OFFSET_USER6

Name: OFFSET_USER6 Address: 125 (7Dh) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	ACCEL_Y_OFFUSER[7:0]	Lower bits of Y-accel offset programmed by user. Max value is ± 64 dps, resolution is 1/32 dps.

17.11 OFFSET_USER7

Name: OFFSET_USER7 Address: 126 (7Eh) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:4	ACCEL_Z_OFFUSER[11:8]	Upper bits of Z-accel offset programmed by user. Max value is ± 64 dps, resolution is 1/32 dps.
3:0	ACCEL_Y_OFFUSER[11:8]	Upper bits of Y-accel offset programmed by user. Max value is ± 64 dps, resolution is 1/32 dps.

17.12 OFFSET_USER8

Name: OFFSET_USER8 Address: 127 (7Fh) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	NAME	FUNCTION
7:0	ACCEL_Z_OFFUSER[7:0]	Lower bits of Z-accel offset programmed by user. Max value is ± 64 dps, resolution is 1/32 dps.

18 REFERENCE

Please refer to “InvenSense MEMS Handling Application Note (AN-IVS-0002A-00)” for the following information:

- Manufacturing Recommendations
 - Assembly Guidelines and Recommendations
 - PCB Design Guidelines and Recommendations
 - MEMS Handling Instructions
 - ESD Considerations
 - Reflow Specification
 - Storage Specifications
 - Package Marking Specification
 - Tape & Reel Specification
 - Reel & Pizza Box Label
 - Packaging
 - Representative Shipping Carton Label
- Compliance
 - Environmental Compliance
 - DRC Compliance
 - Compliance Declaration Disclaimer

19 DOCUMENT INFORMATION

19.1 REVISION HISTORY

Revision Date	Revision	Description
09/25/2018	0.1	Initial Release
10/04/2018	0.2	Updated Section 3
10/10/2018	0.3	Updated Section 13
11/05/2018	0.4	Added Section 11; Updated Sections 13, 14, 15
12/05/2018	0.5	Updated Section 3
12/07/2018	0.6	Updated Section 3
12/17/2018	0.7	Updated Section 11
03/26/2019	0.8	Updated Section 5

This information furnished by InvenSense, Inc. ("InvenSense") is believed to be accurate and reliable. However, no responsibility is assumed by InvenSense for its use, or for any infringements of patents or other rights of third parties that may result from its use. Specifications are subject to change without notice. InvenSense reserves the right to make changes to this product, including its circuits and software, in order to improve its design and/or performance, without prior notice. InvenSense makes no warranties, neither expressed nor implied, regarding the information and specifications contained in this document. InvenSense assumes no responsibility for any claims or damages arising from information contained in this document, or from the use of products and services detailed therein. This includes, but is not limited to, claims or damages based on the infringement of patents, copyrights, mask work and/or other intellectual property rights.

Certain intellectual property owned by InvenSense and described in this document is patent protected. No license is granted by implication or otherwise under any patent or patent rights of InvenSense. This publication supersedes and replaces all information previously supplied. Trademarks that are registered trademarks are the property of their respective companies. InvenSense sensors should not be used or sold in the development, storage, production or utilization of any conventional or mass-destructive weapons or for any other weapons or life threatening applications, as well as in any other life critical applications such as medical equipment, transportation, aerospace and nuclear instruments, undersea equipment, power plant equipment, disaster prevention and crime prevention equipment.

©2019 InvenSense. All rights reserved. InvenSense, MotionTracking, MotionProcessing, MotionProcessor, MotionFusion, MotionApps, DMP, AAR, and the InvenSense logo are trademarks of InvenSense, Inc. The TDK logo is a trademark of TDK Corporation. Other company and product names may be trademarks of the respective companies with which they are associated.



©2019 InvenSense. All rights reserved.

单击下面可查看定价，库存，交付和生命周期等信息

[>>InvenSense / TDK](#)